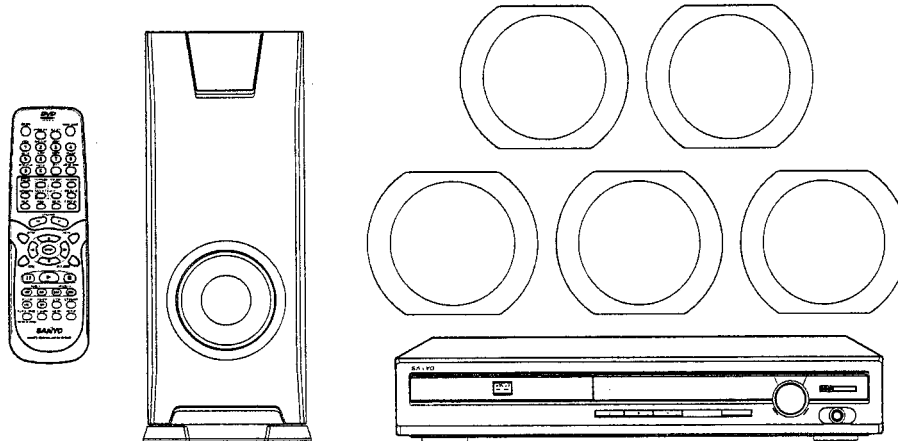


## Service Manual

## DVD Home Theater System

DC-TS755KR (KR)



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PRODUCT CODE No.  
129 636 05

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## SPECIFICATIONS

### Amplifier

#### Main amplifier

Stereo mode  
26W x 2  
(at 8 ohms, 10% distortion)

#### Dolby Digital mode

26W x 2  
(at 8 ohms, 10% distortion, with Centre/Surround/Subwoofer amplifier off)

#### Centre amplifier

26W  
(at 8 ohms, 10% distortion, with Main/Surround/Subwoofer amplifier off)

#### Surround amplifier

26W x 2  
(at 8 ohms, 10% distortion, with Main/Center/Subwoofer amplifier off)

#### Subwoofer amplifier

50 W  
(at 4 ohms, 10% distortion, with Main/Center/Surround amplifier off)  
US is Active Subwoofer.

#### Input:

VIDEO (AUDIO) IN 1: 500 mV/50 k $\Omega$   
VIDEO (AUDIO) IN 2: 500 mV/50 k $\Omega$

#### Outputs:

**SPEAKERS:**  
FRONT (L/R): 8  $\Omega$   
CENTER: 8  $\Omega$   
SURROUND (L/R): 8  $\Omega$   
SUBWOOFER: 4  $\Omega$

#### MONITOR OUT:

S-VIDEO:  
Y: 1.0 Vp-p (75  $\Omega$ )  
C: 0.286 Vp-p (75  $\Omega$ ) NTSC, 0.3 Vp-p (75  $\Omega$ ) PAL  
VIDEO: 1.0 Vp-p (75  $\Omega$ )

### DVD Player

#### Type:

DVD video player

#### Playback standard:

PAL or NTSC

#### Laser:

Semiconductor laser, wavelength: 650/790 nm  
Laser output (Continuous wave max.):  
1 mW (DVD)  
0.5 mW (CD)

#### Signal to noise ratio:

More than 105 dB

#### Harmonic distortion

0.003 %

#### Wow and flutter:

Below measurable level

### Tuner

#### Reception frequency:

FM: 87.5 - 108 MHz  
AM: 522 - 1,710 kHz

### General

#### Power requirements:

AC 220 V, 60 Hz

#### Power consumption:

120 W

#### Dimensions:

435(W) x 75(H) x 375(D) mm

#### Weight:

6.4 kg

### Speaker system

Front left, Front right, Centre, Surround left and Surround right speakers (SX-TS750S, magnetic shield)

#### Unit used:

8 cm cone type, full range

#### Maximum power handling capacity:

40 W (peak)

#### Nominal impedance:

8  $\Omega$

#### Dimensions:

125(W) x 105(H) x 112(D) mm

#### Weight:

0.72 kg/speaker

#### Subwoofer (SX-TS750W)

#### Unit used:

13 cm cone type

#### Maximum power handling capacity:

80 W (peak)

#### Nominal impedance:

4  $\Omega$

#### Dimensions:

160(W) x 415(H) x 310(D) mm

#### Weight:

4.9 kg

Specifications subject to change without notice.

## LASER BEAM SAFETY PRECAUTION

- Pick-up that emits a laser beam is used in this CD player section.

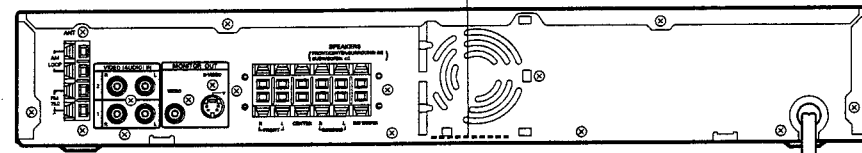
### CAUTION :

USE OF CONTROLS OR ADJUSTMENTS  
OR PERFORMANCE OF PROCEDURES  
OTHER THAN THOSE SPECIFIED HEREIN  
MAY RESULT IN HAZARDOUS RADIATION  
EXPOSURE

LASER OUTPUT ..... 0.6 mW Max. (CW)

WAVELENGTH ..... 790 nm

CAUTION - INVISIBLE LASER RADIATION WHEN OPEN AND  
INTERLOCKS DEFEATED. AVOID EXPOSURE TO BEAM.  
ADVARSEL - USYNLIG LASER STRÅLING VED ÅBNING, NÅR  
SIKKERHEDSAFBRYDERE ER UDE AF FUNKTION, UDGÅ UDS ÆTTELSE  
FOR STRÅLING.  
VARNING - OSYNLIG LASER STRÅLING NÅR DENNA DEL ÄR ÖPPNAD  
OCH SPÄRR ÄR URKOPPLAD. STRÅLEN ÄR FARLIG.  
VORSICHT - UNSICHTBARE LASERSTRAHLUNG TRIT AUS, WENN  
DECKEL GEÖFFNET UND WENN SICHERHEITSVERRIEGELUNG  
ÜBERBRÜCKT IST. NICHT, DEM STRAHL AUSSETZEN.  
VARO - AVATTAESSA JA SUOJALUKITUS OHITETTAESSA OLET ALLTIINA  
NÄKYMÄTTÖMÄLLE LASERSÄTEILYLLE. ÄLÄ KATSO SÄTEESEEN.



## DVD MECHANISM REPLACEMENT

### 1. Cautionary instructions in handling the assy

#### (Safety instructions)

#### Optical pickup

The laser beam used in the pickup is classified as "class 2".  
Exposing your eyes or skin to the beam is harmful. Take care  
not to do so.

#### (Caution against static electricity and leakage voltage)

Ground securely the work tables, tools, fixtures, soldering irons  
(including those made of ceramic) and measuring instruments  
used in the production lines and inspection departments that  
handle loaders. The workers shall also be grounded.

#### (Cautionary instructions in handling)

Do not touch the object lens when handling a loader, or the lens  
will be stained, resulting in inadequate playability.

There is no power supply protection circuit provided for this  
product or adjustment/inspection device. Short-circuiting may  
lead to fire or damage.

Take care so as to protect from exposure to water, the entry of  
metallic pieces or dew condensation.

In particular, a strong magnet adjacent to the pickup will not  
only get inoperative but can damage the pickup if a small metallic  
piece, such as a screw or swarm, enters.

The loader edge can cause injury if inadvertently handled.

Do not touch a rotating disk, or injury may result.

This product is a precision device. Handle carefully.

A shock or dropping will cause misalignment or destruction. If it  
should occur, refer to clause 2.

This product is so designed as to endure an initial shock  
equivalent to a drop from a height of approx. 90 cm under the  
packed condition.

After the initial shock, the resistivity will still remain at a level of  
50 to 60 G, but the mechanical robustness will weaken.

Do not place in a dusty location.

The entry and deposition of dirt into or on the pickup lens or  
moving section will cause malfunction or degradation.

#### (Connectors)

Do not connect or disconnect while power is on.  
Connecting or disconnecting signal wires or the main power cord  
when the power is on may destruct the unit or fixture.

When connecting, push all the way in securely.  
An insufficient insertion may cause a bad contact, leading to an  
erroneous operation.

Do not connect or disconnect roughly by an excessively strong  
force, or a broken wire or bad contact may result.

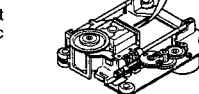
Semiconductors are connected. Do not touch connector terminals  
directly.

If the worker is grounded, there is nothing to worry about static  
electricity, but the rust on the connector terminal surface caused  
by the touch may result in bad contact.

#### (Caution)

Before disconnecting FFC  
cable, make it "SHORT" as  
shown left.

After connecting FFC  
cable, make it "OPEN" as  
shown left.



#### (Power source)

The power source need be good in quality (free from  
instantaneous interruptions or noises).

A low quality power source may well cause malfunction.

#### (Storage)

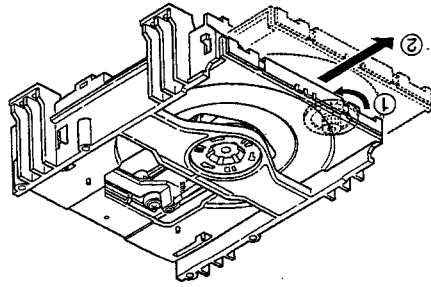
Do not place or store in a dusty place or a place where dew  
condensation is possible.

The entry and deposition of dirt or dust into or on the pickup lens  
or moving section will cause malfunction or degradation.

Also, dew condensation causes rust; the rust penetrate into the  
precision part of a pickup, causing malfunction, or degrading the  
optical quality of the internal lens and reflector, which also leads  
to malfunction.

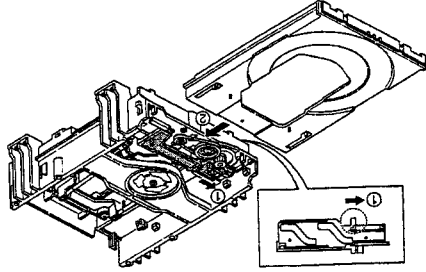
# MECHANISM REPLACEMENT

1. How to remove the tray.



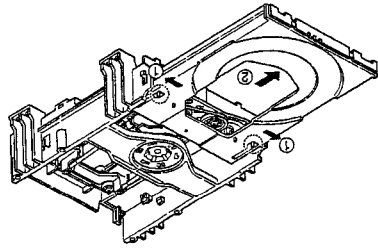
Rotate the ① gear.  
Move forward the ② tray.

2. How to insert the tray.

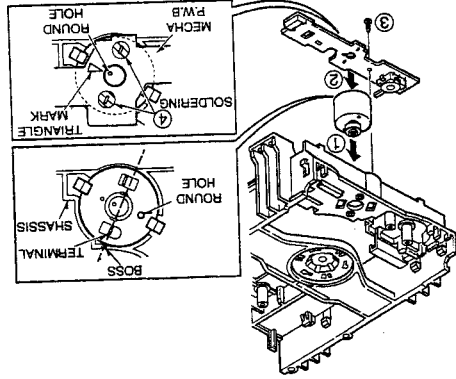


Move the ① slide to the left end.  
Insert the ② tray.

3. How to install the motor.



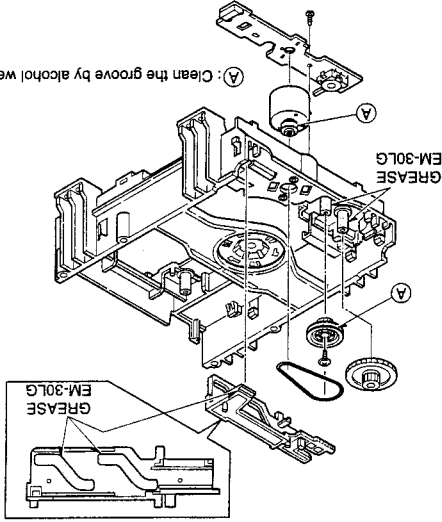
Move both the right and left ① tray pins to the ends.  
Remove the ② tray.



① Adjust the motor terminal to boss in the chassis.  
② Adjust the round hole of the motor to the triangle mark of P.W.B, and solder it.

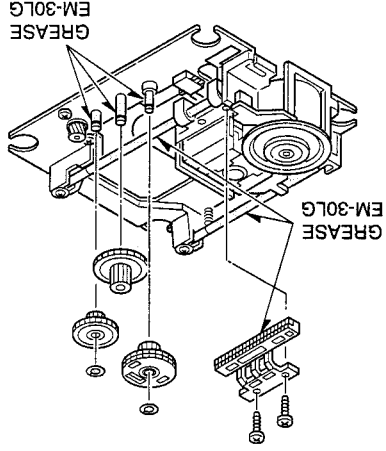
# MECHANISM REPLACEMENT

4. Base mechanism mounting parts.

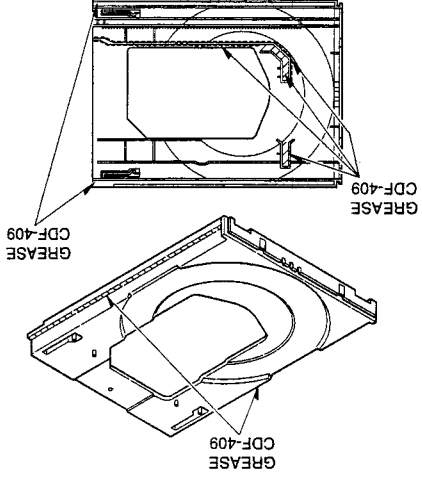


① Clean the groove by alcohol well.

5. Base mechanism parts.



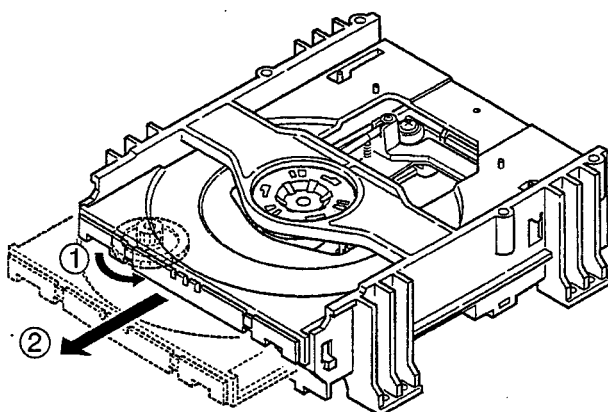
6. Tray parts.



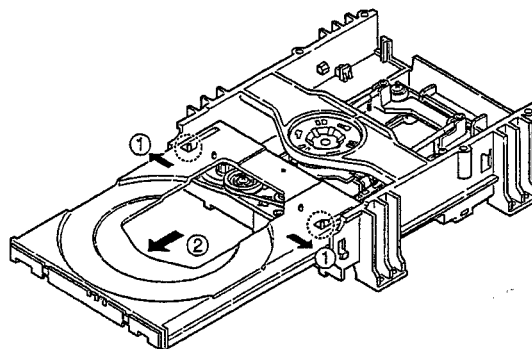
Do not remove the pick-up from base mechanism because of adjustment difficulty.

## MECHANISM REPLACEMENT

### 1. How to remove the tray.

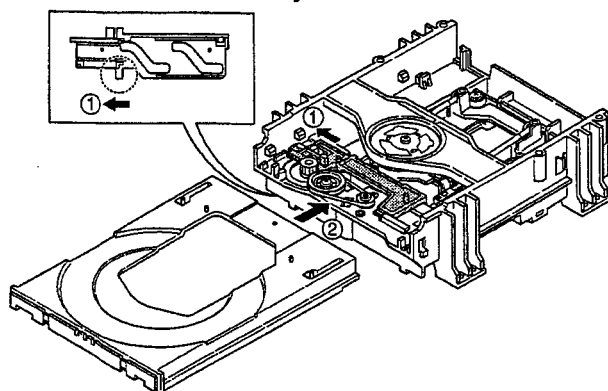


Rotate the ① gear.  
Move forward the ② tray.



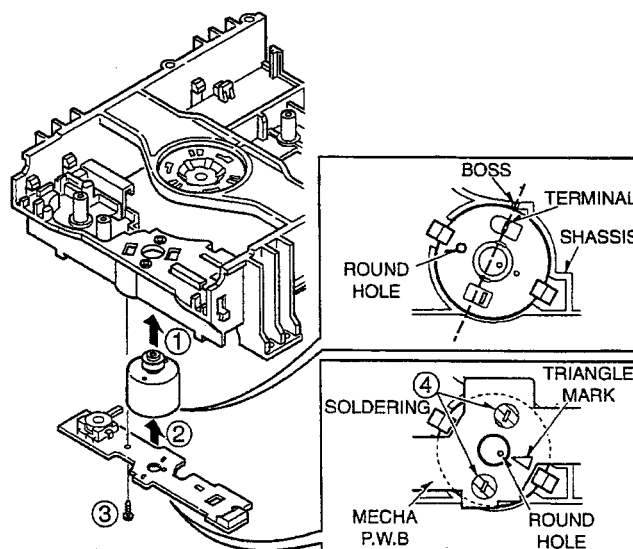
Move both the right and left ① tray pins to the ends.  
Remove the ② tray.

### 2. How to insert the tray.



Move the ① slide to the left end.  
Insert the ② tray.

### 3. How to install the motor.

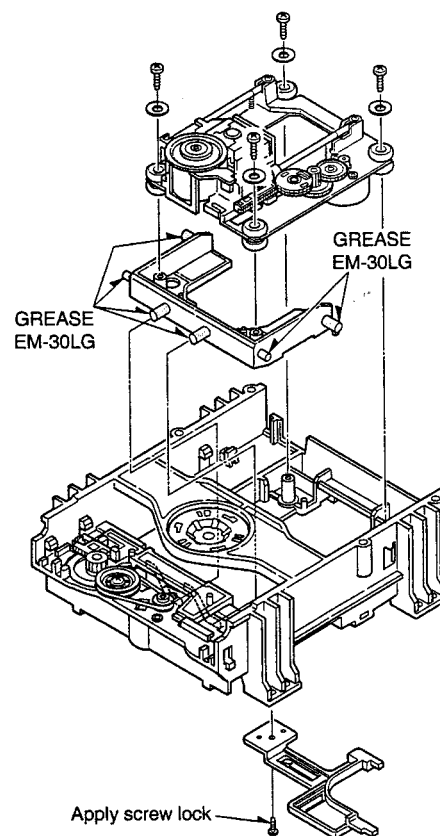
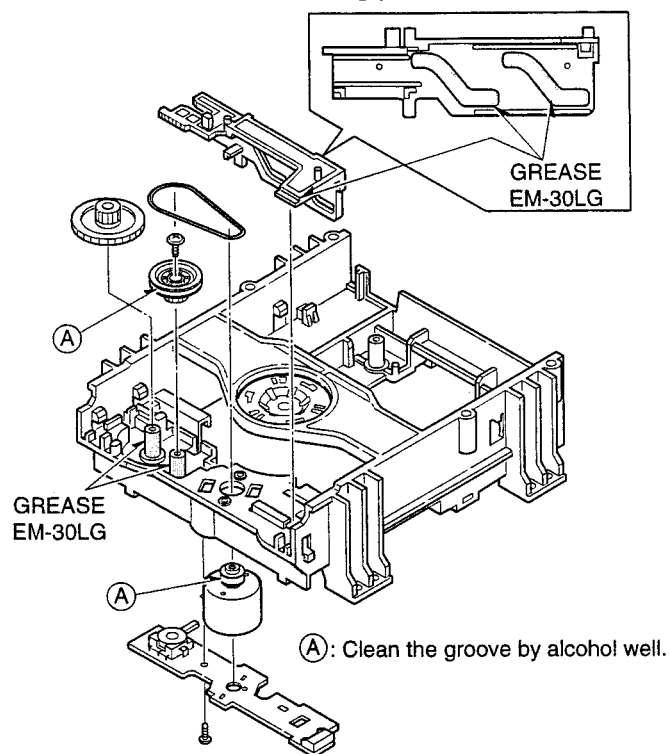


- ① Adjust the motor terminal to boss in the chassis.
- ② Adjust the round hole of the motor to the triangle mark of P.W.B, and solder it.

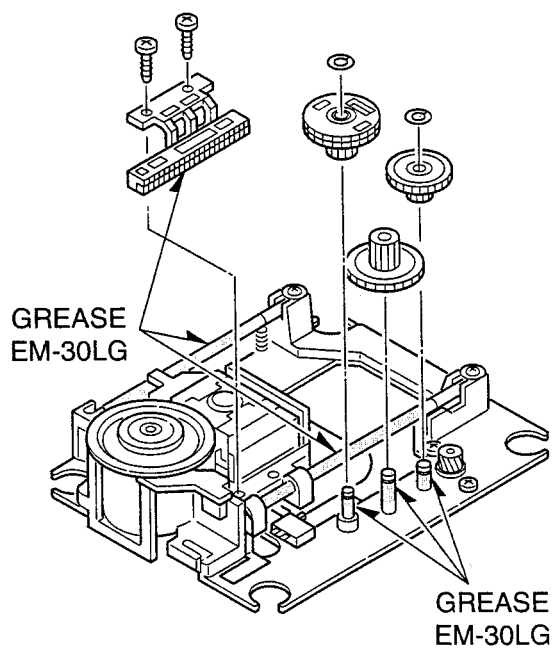


## MECHANISM REPLACEMENT

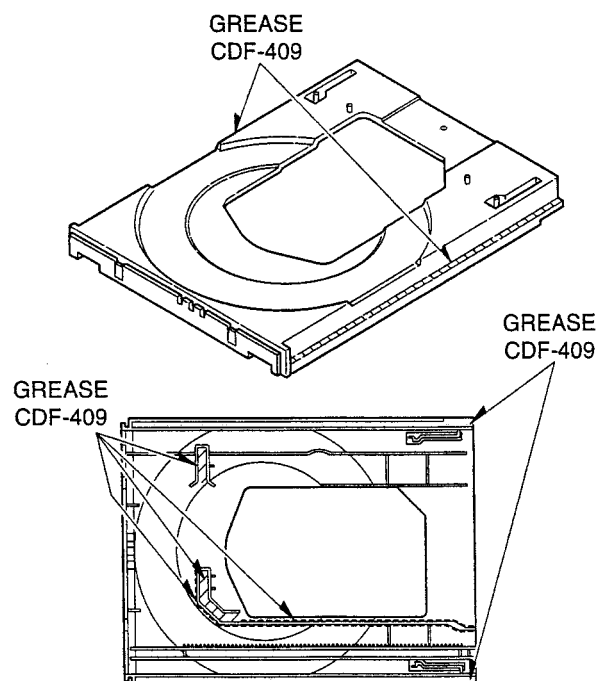
### 4. Base mechanism mounting parts.



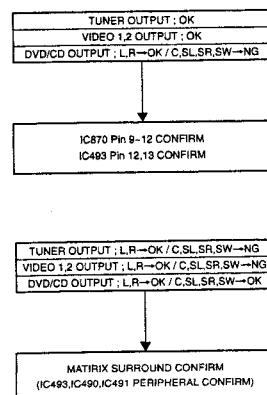
### 5. Base mechanism parts.



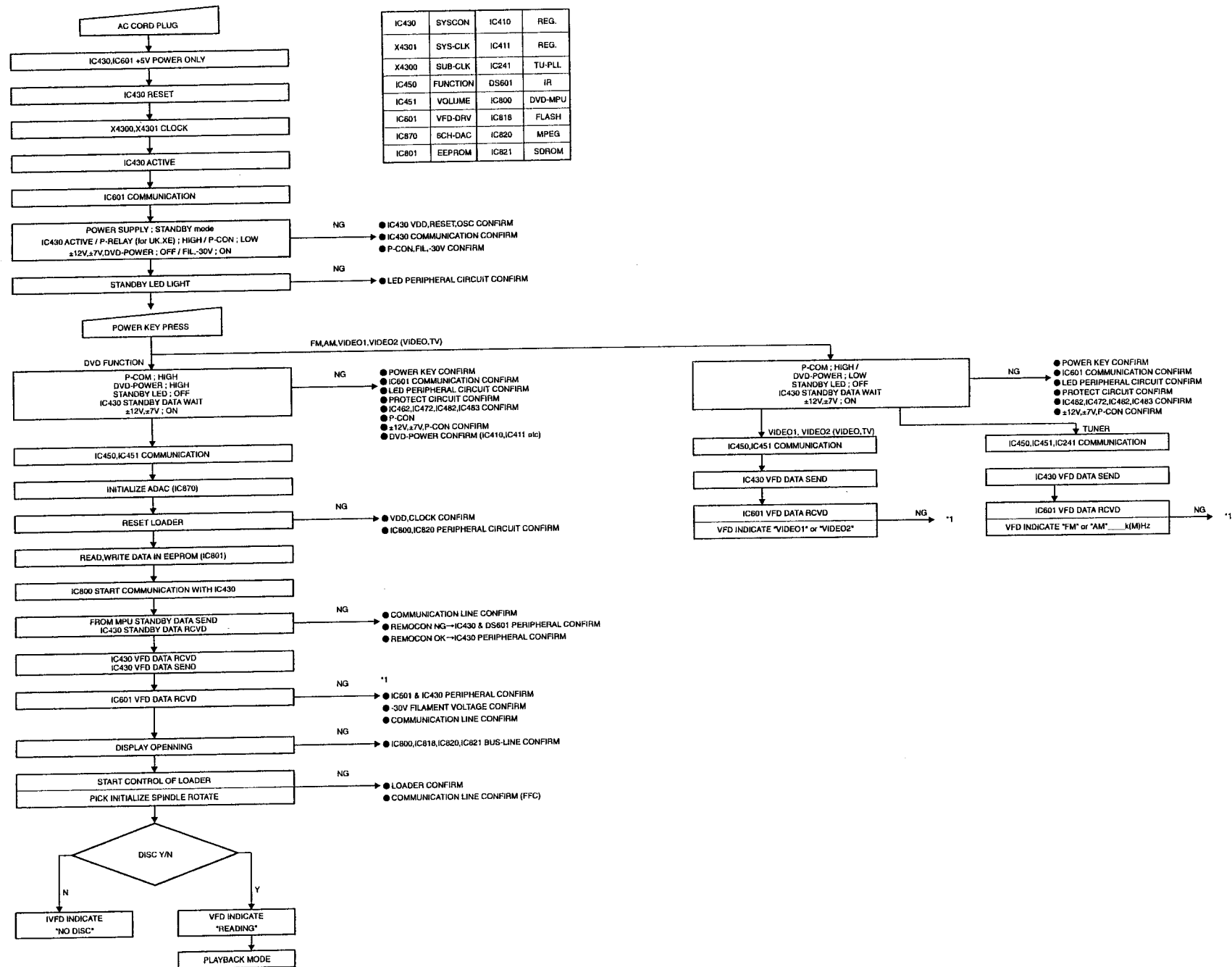
### 6. Tray parts.

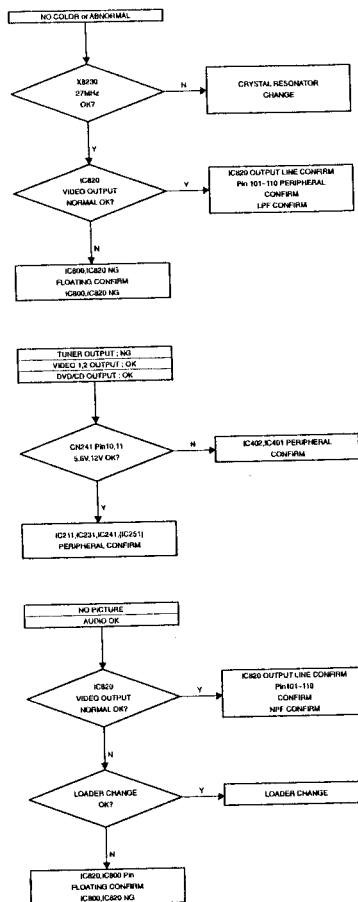


Do not remove the pick-up from base mechanism because of adjustment difficulty.



- 5 -



**A. Market / Region SETUP**

In the initial condition for this model, Market and Region Information are undefined.

In the following cases, be sure to set up Market/Region.

1. When updating the system using CD-R

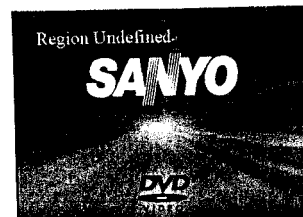
(Part code : 0PRADC9635--AC).

2. When replacing a DVD substrate.

While Market/Region information are undefined, the message

"Region Undefined" is displayed on the screen.

NOTE: Even if the condition is not under 1 or 2 above, if the message "Region Undefined" is displayed, be sure to set up Market/Region.

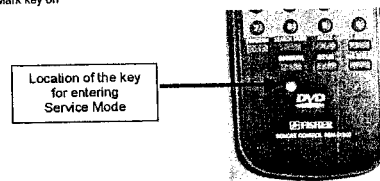


Message under the Market/Region undefine condition

**B. How to enter Service Mode.**

You can enter Service Mode in any one of the following ways (1 to 2).

1. Pushing the covered key located beneath Book Mark key on RB-1500 or REM-S1500.



2. Simultaneously pushing both Shift key and ON SCREEN key on RB-TS750SS.

## SERVICE MODE

### C. Setup Procedures

#### 1. Displaying SERVICE MODE screen

Display Service Mode screen following the instructions "How to enter Service Mode" above.



#### 2. Displaying Internal Setup screen

Push NEXT button within three seconds after operating the Service Mode display.

On the Internal Setup screen shown on the right, set up Market and Region.

| Model      | Market | Region |
|------------|--------|--------|
| DC-TS755KR | PDT    | 3      |

Market/Region setup table.

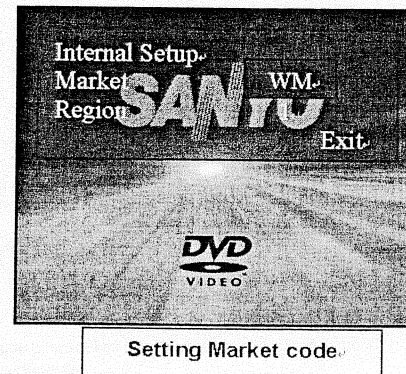


#### 3. Setting Market code

3.1. While a highlighted indicator is displayed on the right side of the Market denotation, push ENT button on the remote controller. With each push the indicator will advance as shown below.

WM -> SFC -> EUR -> S18 -> SS -> PA - - - PDT

3.2. Specify the code of the model in accordance with the Market/Region Setup Table above.



3.3 Once the desired code is displayed, push ▼ button to move the highlighted indicator to the Region input area.

## SERVICE MODE

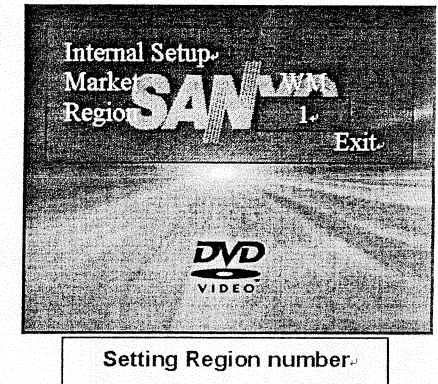
#### 4. Setting REGION code

4.1 While a highlighted indicator is displayed on the right side of the Region denotation, push ENT button on the remote controller. With each push the indicator will advance as shown below.

1 -> 2 -> 3 -> 4 -> 5 -> 6

4.2 Specify the number of the model in accordance with the Market/Region Setup Table above.

4.3 Once the desired number is displayed, push ▼ button to move the highlighted indicator to Exit area.



#### 5. Saving settings

5.1 Make sure that the Market and Region settings are properly set.

(If any of the settings are incorrect, you can make a change by moving the indicator using p button, and following procedures 3 and 4 above.)

5.2 After ensuring that the settings are all correct, push ENT button while the indicator is on Exit area. The settings are now saved.



#### 6. Finishing settings

6.1 After a few seconds, the Internal Setup screen disappears, and then the Service Mode screen is displayed again for three seconds as shown on the right.

You should check the settings.

Backend version S 11225 A 0  
 Brand (S : SANYO , F : FISHER)  
 Version ( 2 0 0 1 , 12 , 25)  
 Sub Version (A,B,.....Z)  
 Region ( 0 : Region undefined  
 1 ~ 6 : Region defined  
 F : Region Free )



6.2 Power OFF.

## SERVICE MODE

### D. IMPORTANT NOTE

- Once the "Market/Region" settings are written into EEPROM (IC801) on the DVD substrate, they cannot be reset.  
(However, updating the system using CD-R enables you to make new settings.)
- While the Internal Setup screen is displayed, pushing the Power button enables you to terminate the operations without

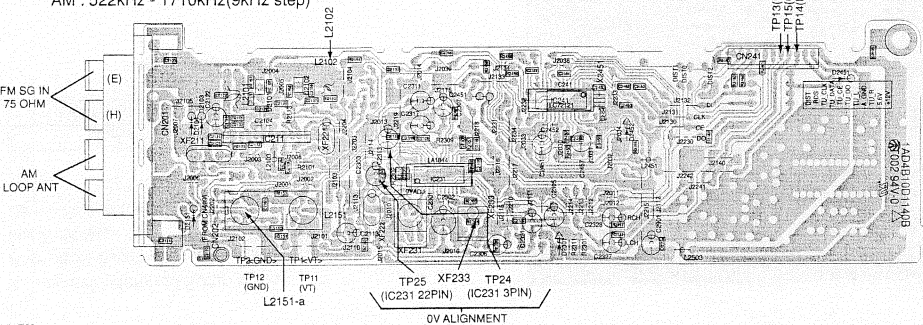
## HOW TO LOAD SOFTWARE FOR MPEG P.W.BOARD

- Power on, then open tray.
- It take on CD-ROM for UPDATE software to the tray, and tray close.
- Display "UP DATE" in the TV screen.
- For the time being, tray open and FL display remain "UP DATE".
- When software loading finished, FL display "STANDBY".
- Next, set up market code and region code by "SERVICE MODE"  
CD-ROM part code is "OPRADC9635--AC".

## TUNER ADJUSTMENTS

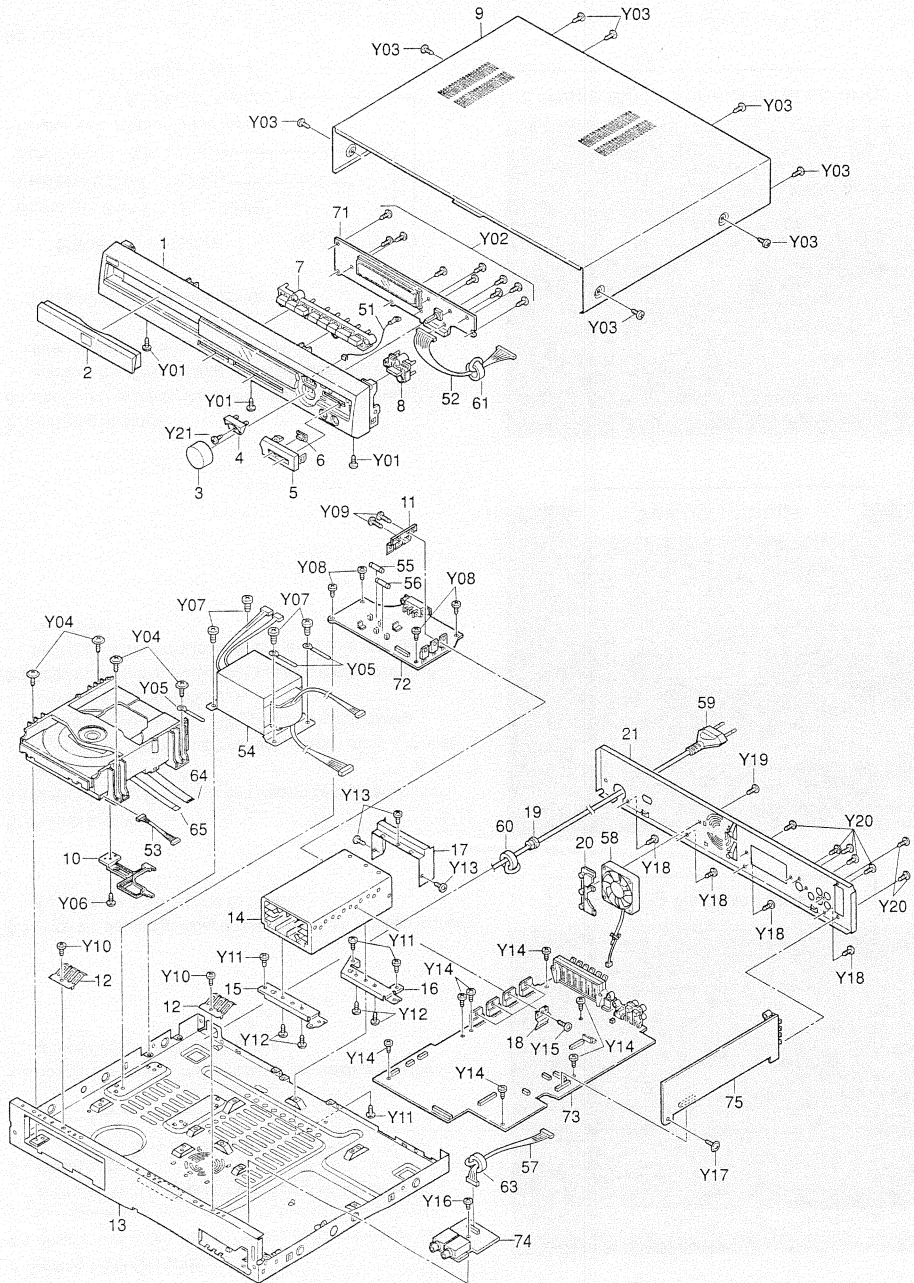
- Use a plastic screw driver for adjustments.
- MODE : STEREO
- Speaker impedance : 8  $\Omega$
- TUNING
  - FM : 87.5MHz - 108MHz(50kHz step)
  - AM : 522kHz - 1710kHz(9kHz step)

SG RF Level : 75 $\Omega$  open Voltage dB $\mu$ V  
Antenna : 75 $\Omega$  unbalanced Direct, Modulation : 1 kHz  
Dev. :  $\pm 22.5$ kHz(MONO)  $\pm 22.5$ kHz(STEREO)  
 $\pm 6.75$ kHz(PILOT)  
Output Level : about 100mV at TP13, TP14, TP15



| 1. FM |                   |                                                  |                                                   |              |              |            |                                                 |
|-------|-------------------|--------------------------------------------------|---------------------------------------------------|--------------|--------------|------------|-------------------------------------------------|
| Step  | Adjusting Circuit | Connection                                       |                                                   | SG Frequency | Set Position | Adjustment | Remark                                          |
|       |                   | Input                                            | Output                                            |              |              |            |                                                 |
| 1     | IF Alignment      | FM ANT.<br>SG=66dB $\mu$ V                       | IC231 3,22pin<br>TP24, TP25                       | 98MHz        | ---          | XF233      | 0.0 $\pm$ 0.05V                                 |
| 2     | Cover voltage     | ---                                              | Connect Digital DC voltmeter to TP11(H), TP12(E). | 87.5MHz      | Low          | L2102      | Alignment voltage of 87.9MHz is 1.1 $\pm$ 0.1V. |
|       |                   | ---                                              |                                                   | 108MHz       | High         |            | Confirm voltage of 107.9MHz is <9.0V.           |
| 3     | Tracking          | Connect FM SG to FM Antenna (SG=8dB $\mu$ V)     | Connect to VTVM TP13(L) or TP14(R), TP15(E)       | 90MHz        | Low          | L2101      | Max.                                            |
|       |                   |                                                  |                                                   | 106MHz       | High         |            |                                                 |
| 2. AM |                   |                                                  |                                                   |              |              |            |                                                 |
| Step  | Adjusting Circuit | Connection                                       |                                                   | SG Frequency | Set Position | Adjustment | Remark                                          |
|       |                   | Input                                            | Output                                            |              |              |            |                                                 |
| 1     | Cover voltage     | ---                                              | Connect Digital DC voltmeter to TP11(H), TP12(E). | 522kHz       | Low          | ---        | more than 0.8V                                  |
|       |                   | ---                                              |                                                   | 1710 kHz     | High         | ---        | less than 9.0V                                  |
| 2     | Tracking          | Connect AM SG to Test loop Ant.(SG=80dB $\mu$ V) | Connect to VTVM TP13(L) or TP14(R), TP15(E).      | 603kHz       | Low          | L2151-a    | Max.                                            |
|       |                   |                                                  |                                                   | 1404kHz      | High         |            |                                                 |

## EXPLODED VIEW (CABINET & CHASSIS)





## SERVICE MODE

### D. IMPORTANT NOTE

- Once the "Market/Region" settings are written into EEPROM (IC801) on the DVD substrate, they cannot be reset.  
(However, updating the system using CD-R enables you to make new settings.)
- While the Internal Setup screen is displayed, pushing the Power button enables you to terminate the operations without

## HOW TO LOAD SOFTWARE FOR MPEG P.W.BOARD

- Power on, then open tray.
- It take on CD-ROM for UPDATE software to the tray, and tray close.
- Display "UP DATE" in the TV screen.
- For the time being, tray open and FL display remain "UP DATE".
- When software loading finished, FL display "STANDBY".
- Next, set up market code and region code by "SERVICE MODE"  
CD-ROM part code is "0PRADC9635--AC".

## TUNER ADJUSTMENTS

- Use a plastic screw driver for adjustments.
- MODE : STEREO
- Speaker impedance : 8  $\Omega$
- TUNING

FM : 87.5MHz - 108MHz(50kHz step)

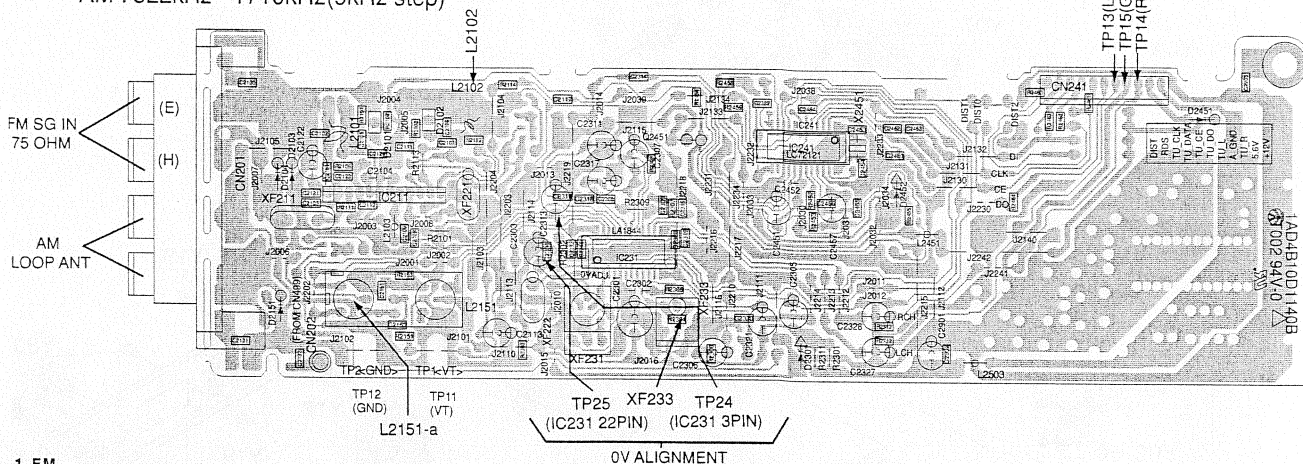
AM : 522kHz - 1710kHz(9kHz step)

SG RF Level : 75 $\Omega$  open Voltage dB $\mu$ V

Antenna : 75 $\Omega$  unbalanced Direct, Modulation : 1 kHz

Dev. :  $\pm 22.5$ kHz(MONO)  $\pm 22.5$ kHz(STEREO)  
 $\pm 6.75$ kHz(PILOT)

Output Level : about 100mV at TP13,TP14,TP15



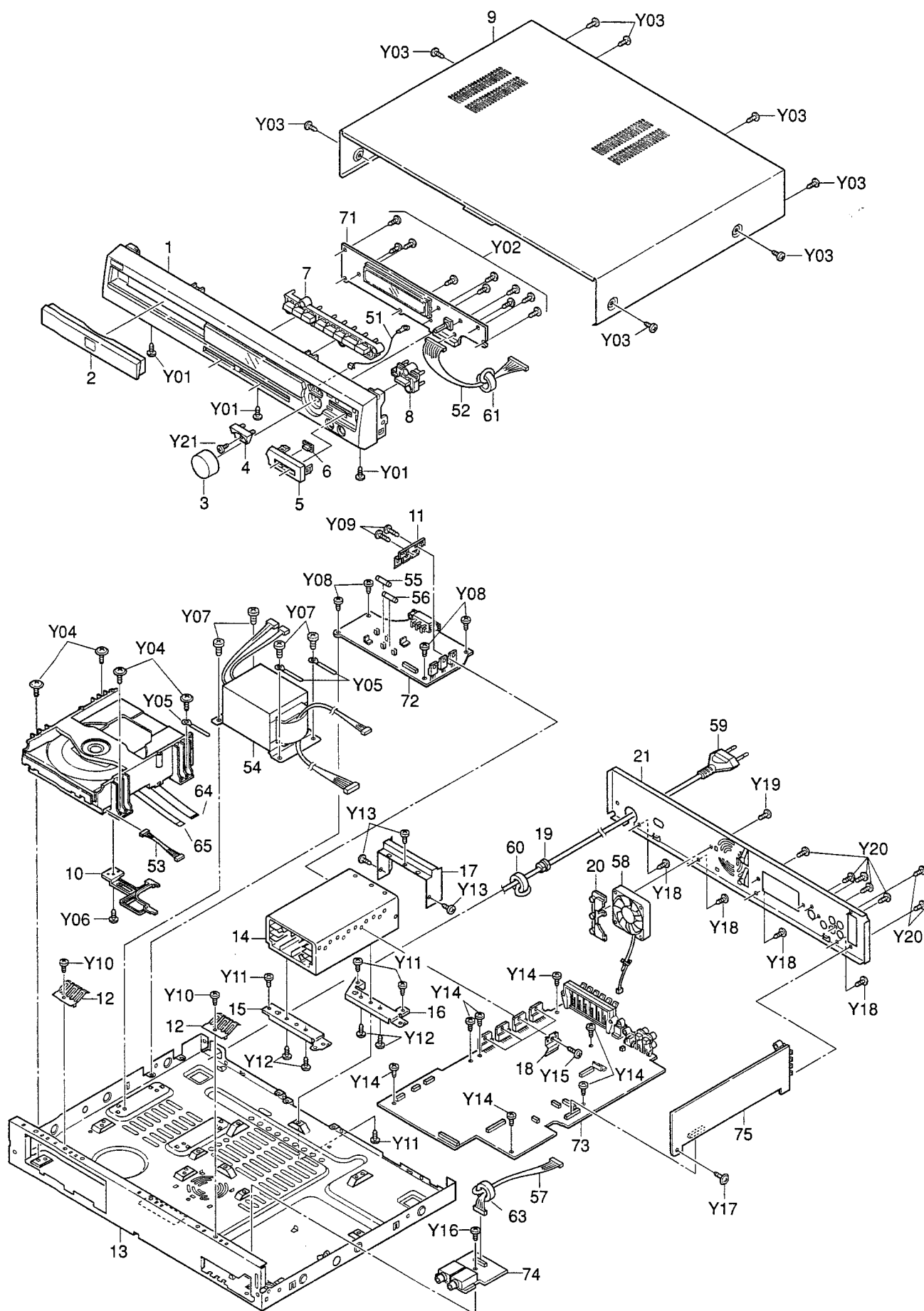
### 1. FM

| Step | Adjusting Circuit | Connection                                   |                                                   | SG Frequency | Set Position | Adjustment | Remark                                          |
|------|-------------------|----------------------------------------------|---------------------------------------------------|--------------|--------------|------------|-------------------------------------------------|
|      |                   | Input                                        | Output                                            |              |              |            |                                                 |
| 1    | IF Alignment      | FM ANT.<br>SG=66dB $\mu$ V                   | IC231 3,22pin<br>TP24, TP25                       | 98MHz        | ---          | XF233      | 0.0 $\pm$ 0.05V                                 |
| 2    | Cover voltage     | ---                                          | Connect Digital DC voltmeter to TP11(H), TP12(E). | 87.5MHz      | Low          | L2102      | Alignment voltage of 87.9MHz is 1.1 $\pm$ 0.1V. |
|      |                   | ---                                          |                                                   | 108MHz       | High         |            | Confirm voltage of 107.9MHz is <9.0V.           |
| 3    | Tracking          | Connect FM SG to FM Antenna (SG=8dB $\mu$ V) | Connect to VTVM TP13(L) or TP14(R), TP15(E)       | 90MHz        | Low          | L2101      | Max.                                            |
|      |                   |                                              |                                                   | 106MHz       | High         |            |                                                 |

### 2. AM

| Step | Adjusting Circuit | Connection                                       |                                                   | SG Frequency | Set Position | Adjustment | Remark         |
|------|-------------------|--------------------------------------------------|---------------------------------------------------|--------------|--------------|------------|----------------|
|      |                   | Input                                            | Output                                            |              |              |            |                |
| 1    | Cover voltage     | ---                                              | Connect Digital DC voltmeter to TP11(H), TP12(E). | 522kHz       | Low          | ---        | more than 0.8V |
|      |                   | ---                                              |                                                   | 1710 kHz     | High         |            | less than 9.0V |
| 2    | Tracking          | Connect AM SG to Test loop Ant.(SG=80dB $\mu$ V) | Connect to VTVM TP13(L) or TP14(R), TP15(E).      | 603kHz       | Low          | L2151-a    | Max.           |
|      |                   |                                                  |                                                   | 1404kHz      | High         |            |                |

# EXPLODED VIEW (CABINET & CHASSIS)





## PARTS LIST

### PRODUCT SAFETY NOTICE

EACH PRECAUTION IN THIS MANUAL SHOULD BE FOLLOWED DURING SERVICING. COMPONENTS IDENTIFIED WITH THE IEC SYMBOL  $\Delta$  IN THE PARTS LIST AND THE SCHEMATIC DIAGRAM DESIGNATED COMPONENTS IN WHICH SAFETY CAN BE OF SPECIAL SIGNIFICANCE. WHEN REPLACING A COMPONENT IDENTIFIED BY  $\Delta$ , USE ONLY THE REPLACEMENT PARTS DESIGNATED, OR PARTS WITH THE SAME RATINGS OF RESISTANCE, WATTAGE OR VOLTAGE THAT ARE DESIGNATED IN THE PARTS LIST IN THIS MANUAL. LEAKAGE-CURRENT OR RESISTANCE MEASUREMENTS MUST BE MADE TO DETERMINE THAT EXPOSED PARTS ARE ACCEPTABLY INSULATED FROM THE SUPPLY CIRCUIT BEFORE RETURNING THE PRODUCT TO THE CUSTOMER.

**CAUTION :** Regular type resistors and capacitors are not listed. To know those values, refer to the schematic diagram.  
Regular type resistors are less than 1/4 W carbon type and chip resistors.  
Regular type capacitors are less than 50 V and less than 1000  $\mu$ F type of Ceramic type and Electrical type.

### PACKING & ACCESSORIES

| REF.NO. | PART NO.     | DESCRIPTION                   | REF.NO. | PART NO.     | DESCRIPTION                     |
|---------|--------------|-------------------------------|---------|--------------|---------------------------------|
|         | 614 324 7173 | CARTON CASE, INNER            | Y11     | 411 021 6405 | EARTH SPRING PLATE              |
|         | 614 322 7847 | CUSHION, LEFT, LEFT           |         |              | SCR S-TPG BIN 3X8,              |
|         | 614 322 7854 | CUSHION, RIGHT, RIGHT         | Y12     | 411 021 6405 | HOLDER H/S-PWB                  |
|         | 614 324 7203 | INSTRUCTION MANUAL            |         |              | SCR S-TPG BIN 3X8,              |
|         | 645 052 1621 | POLY BAG, VIDEO/AUDIO         | Y13     | 411 021 6405 | HOLDER H/S-BOTTOM               |
|         | 645 011 9736 | POLY BAG, INST MANUAL         |         |              | SCR S-TPG BIN 3X8,              |
|         | 645 048 1994 | POLY SHEET, SET               | Y14     | 411 021 6405 | COVER FAN-HEAT SINK             |
|         | 645 043 9735 | BATTERY COVER, SERVICE PART   | Y15     | 411 021 6405 | SCR S-TPG BIN 3X8, MAIN PWB     |
|         | 645 048 5053 | BATTERY COVER                 | Y16     | 411 021 6405 | SCR S-TPG BIN 3X8, IC-HEAT SINK |
|         | 614 324 7050 | ASSY, BOX, SPEAKER, SATELLITE | Y17     | 411 020 9902 | SCR S-TPG BRZ-FLG 3X8, TUN PWB  |
|         | 614 324 7067 | ASSY, BOX, SPEAKER, WOOFER    | Y18     | 411 021 3701 | SCR S-TPG BIN 3X10,             |
|         | 645 005 1227 | ASSY, ANTENNA, LOOP           |         |              | BOTTOM-REAR                     |
|         | 614 245 0055 | ANTENNA                       | Y19     | 411 021 3701 | SCR S-TPG BIN 3X10,             |
|         | 645 041 1373 | CABLE, VIDEO                  | Y20     | 411 021 3701 | MOUNTING FAN-REAR               |
|         | 645 053 5345 | REMOCON, RB-TS750SS           |         |              | SCR S-TPG BIN 3X10,             |
|         |              |                               | Y21     | 411 165 3803 | REAR-ELECT PART                 |
|         |              |                               |         |              | SCR S-TPG BIN 2.3X10,           |
|         |              |                               |         |              | FRONT-ESC VOL                   |

### CABINET & CHASSIS

| REF.NO. | PART NO.     | DESCRIPTION                     |
|---------|--------------|---------------------------------|
| 1       | 614 324 7104 | ASSY, CABINET, FRONT            |
| 2       | 614 322 7700 | ASSY, DEC, DVD TRAY             |
| 3       | 614 322 4839 | KNOB, ROTARY, VOL, VOLUME       |
| 4       | 614 322 4785 | DEC, ESCUTCHEON, VOL            |
| 5       | 614 322 4778 | DEC, ESCUTCHEON, POWER          |
| 6       | 614 322 4761 | DEC, WINDOW, STANDBY, STANDBY   |
| 7       | 614 323 9116 | BUTTON, PLAY, PLAY/FUNCTION     |
| 8       | 614 322 4693 | BUTTON, POWER, POWER SW         |
| 9       | 614 322 7625 | ASSY, CABINET, BENDING,         |
|         |              | AFTER BENDING                   |
| 10      | 614 322 5997 | MOUNTING, FFC, MOUNTING         |
| 11      | 614 291 6568 | MOUNTING, PWB, IC-HEAT SINK     |
| 12      | 614 313 6545 | SPRING, PLATE, EARTH            |
| 13      | 614 322 7694 | ASSY, CABINET, BOTTOM           |
| 14      | 614 322 4808 | HEAT SINK                       |
| 15      | 614 322 4822 | HOLDER, BOTTOM, HEAT SINK       |
| 16      | 614 322 4815 | HOLDER, H/SINK, REAR, HEAT SINK |
| 17      | 614 322 4730 | COVER, FAN, REAR, FAN           |
| 18      | 614 316 1417 | MOUNTING, IC, IC-HEAT SINK      |
| 19      | 614 129 1901 | FIXER, AC CORD                  |
| or      | 614 284 1884 | FIXER, AC CORD                  |
| 20      | 614 310 3837 | MOUNTING, FAN, FAN              |
| 21      | 614 324 3151 | PANEL, REAR, REAR               |

### FIXING PARTS

| REF.NO. | PART NO.     | DESCRIPTION                   |
|---------|--------------|-------------------------------|
| Y01     | 411 021 6405 | SCR S-TPG BIN 3X8,            |
|         |              | FRONT-BOTTOM FIX              |
| Y02     | 411 165 3803 | SCR S-TPG BIN 2.3X10,         |
|         |              | FRONT-PWB FIX                 |
| Y03     | 411 098 4205 | SCR S-TPG BIN 3X8, CABINET    |
| Y04     | 411 020 9803 | SCR S-TPG BRZ-FLG 3X6,        |
|         |              | DVD MECHA                     |
| Y05     | 614 129 9082 | LUG                           |
| Y06     | 411 021 2704 | SCR S-TPG BIN 2.6X6, MOUNTING |
| Y07     | 411 001 3905 | SCR S-TPG BIN 4X6, PT         |
| Y08     | 411 021 6405 | SCR S-TPG BIN 3X8, POWER PWB  |
| Y09     | 411 021 6405 | SCR S-TPG BIN 3X8,            |
|         |              | HOLDER H/S-HEAT SINK          |
| Y10     | 411 021 6405 | SCR S-TPG BIN 3X8,            |

## PARTS LIST

| REF.NO. | PART NO.     | DESCRIPTION        | REF.NO. | PART NO.              | DESCRIPTION             |
|---------|--------------|--------------------|---------|-----------------------|-------------------------|
| S6041   | 645 006 5958 | SWITCH, PUSH 1P-1T | C4103   | 403 325 0302          | ELECT 2200U M 25V       |
| or      | 614 220 5471 | SWITCH, TACT       | C4108   | 403 325 9701          | ELECT 4700U M 25V       |
| or      | 614 240 1002 | SWITCH, TACT       | C4109   | 403 325 2306          | ELECT 4700U M 35V       |
| S6042   | 645 006 5958 | SWITCH, PUSH 1P-1T | C4110   | 403 325 2306          | ELECT 4700U M 35V       |
| or      | 614 220 5471 | SWITCH, TACT       | C4120   | $\Delta$ 403 370 7004 | ELECT 330U M 6.3V       |
| or      | 614 240 1002 | SWITCH, TACT       | C4128   | $\Delta$ 403 373 8404 | ELECT 220U M 10V        |
| S6043   | 645 006 5958 | SWITCH, PUSH 1P-1T | C4130   | $\Delta$ 403 373 9302 | ELECT 100U M 25V        |
| or      | 614 220 5471 | SWITCH, TACT       | C4199   | 403 359 3805          | ELECT 2200U M 10V       |
| or      | 614 240 1002 | SWITCH, TACT       | or      | 403 359 3805          | ELECT 2200U M 10V       |
| S6046   | 645 006 5958 | SWITCH, PUSH 1P-1T | or      | 403 330 2001          | ELECT 2200U M 16V       |
| or      | 614 220 5471 | SWITCH, TACT       | C4301   | 403 325 0401          | ELECT 1000U M 6.3V      |
| or      | 614 240 1002 | SWITCH, TACT       | C4307   | $\Delta$ 403 305 1602 | CERAMIC 27P J 50V       |
| S6047   | 645 006 5958 | SWITCH, PUSH 1P-1T | C4308   | $\Delta$ 403 305 1503 | CERAMIC 22P J 50V       |
| or      | 614 220 5471 | SWITCH, TACT       | C4648   | 403 184 9805          | MT-POLYEST 0.22U J 50V  |
| or      | 614 240 1002 | SWITCH, TACT       | C4649   | 403 184 9805          | MT-POLYEST 0.22U J 50V  |
| S6048   | 645 006 5958 | SWITCH, PUSH 1P-1T | C4651   | 403 184 9805          | MT-POLYEST 0.22U J 50V  |
| or      | 614 220 5471 | SWITCH, TACT       | C4652   | 403 184 9805          | MT-POLYEST 0.22U J 50V  |
| or      | 614 240 1002 | SWITCH, TACT       | C4653   | 403 184 9300          | MT-POLYEST 0.047U J 50V |
| S6049   | 645 006 5958 | SWITCH, PUSH 1P-1T | C4654   | 403 184 9300          | MT-POLYEST 0.047U J 50V |
| or      | 614 220 5471 | SWITCH, TACT       | C4748   | 403 184 9805          | MT-POLYEST 0.22U J 50V  |
| or      | 614 240 1002 | SWITCH, TACT       | C4749   | 403 184 9805          | MT-POLYEST 0.22U J 50V  |
| S6050   | 645 006 5958 | SWITCH, PUSH 1P-1T | C4751   | 403 184 9805          | MT-POLYEST 0.22U J 50V  |
| or      | 614 220 5471 | SWITCH, TACT       | C4752   | 403 184 9805          | MT-POLYEST 0.22U J 50V  |
| or      | 614 240 1002 | SWITCH, TACT       | C4755   | $\Delta$ 403 374 0001 | ELECT 33U M 35V         |
| S6060   | 614 215 9828 | SWITCH, TACT       | C4756   | $\Delta$ 403 374 0001 | ELECT 33U M 35V         |
| or      | 645 035 9224 | SWITCH, PUSH 1P-1T | C4848   | 403 184 9805          | MT-POLYEST 0.22U J 50V  |

### POWER SUPPLY P.W.BOARD ASSY

| REF.NO. | PART NO.              | DESCRIPTION                 | REF.NO. | PART NO.              | DESCRIPTION             |
|---------|-----------------------|-----------------------------|---------|-----------------------|-------------------------|
| 72      | 614 324 0655          | ASSY, PWB, DG(Only initial) | C4854   | 403 184 9300          | MT-POLYEST 0.047U J 50V |
| CN401   | 614 310 2519          | PLUG, 10P                   | C4856   | $\Delta$ 403 374 0001 | ELECT 33U M 35V         |
| or      | 645 005 8158          | PLUG, 10P                   | C4857   | $\Delta$ 403 374 0001 | ELECT 33U M 35V         |
| CN402   | 645 005 9315          | PLUG, 2P                    | C8231   | $\Delta$ 403 305 1404 | CERAMIC 18P J 50V       |
| D4005   | 407 099 4603          | ZENER DIODE MTZJ3.9B        | C8232   | $\Delta$ 403 305 1404 | CERAMIC 18P J 50V       |
| D4008   | 407 099 6102          | ZENER DIODE MTZJ10B         | C8535   | $\Delta$ 403 373 7902 | ELECT 150U M 6.3V       |
| D4009   | 407 012 4406          | DIODE 1SS133                | CN100   | 645 037 6207          | SOCKET, FFC 24P         |
| D4010   | 407 012 4406          | DIODE 1SS133                | CN160   | 614 310 2465          | PLUG, 5P                |
| D4012   | 407 099 6805          | ZENER DIODE MTZJ13B         | or      | 645 005 9292          | PLUG, 5P                |
| FPC41   | $\Delta$ 645 031 7903 | HOLDER, FUSE                | CN162   | 645 043 8882          | SOCKET, FPC 8P          |
| or      | $\Delta$ 645 006 4760 | HOLDER, FUSE                | CN410   | 645 006 1998          | PLUG, 5P                |
| FPC42   | $\Delta$ 645 031 7903 | HOLDER, FUSE                | CN411   | 645 004 2904          | PLUG, 4P                |
| or      | $\Delta$ 645 006 4760 | HOLDER, FUSE                | CN412   | 614 310 2519          | PLUG, 10P               |
| IC401   | $\Delta$ 409 463 6701 | IC KIA7805API               | or      | 645 005 8158          | PLUG, 10P               |
| IC402   | $\Delta$ 409 521 9705 | IC KIA78R12STU              | CN414   | 614 310 2519          | PLUG, 10P               |
| L4000   | $\Delta$ 645 038 7364 | INDUCTOR, 70U               | or      | 645 005 8158          | PLUG, 10P               |
| PR400   | $\Delta$ 645 042 2515 | PROTECTOR, 0.2A 125V        | CN420   | 614 310 2434          | PLUG, 2P                |
| Q4001   | 405 143 6504          | TR KTA1267-GR               | or      | 645 005 7366          | PLUG, 2P                |
| or      | 405 004 4601          | TR 2SA608-F-SPA             | CN470   | 645 051 9437          | TERMINAL, SP-6P         |
| or      | 405 004 5103          | TR 2SA608-G-SPA             | CN490   | 645 037 3831          | JACK, RCA, VIDEO        |
| or      | 405 006 1806          | TR 2SA933S-R                | CN491   | 645 044 9086          | SOCKET, DIN 4P, S-VIDEO |
| or      | 405 006 1905          | TR 2SA933S-S                | CN492   | 645 053 8346          | JACK, RCA-4P, RCA-4P    |
| Q4002   | 405 143 6504          | TR KTA1267-GR               | CN496   | 614 310 2571          | PLUG, 16P               |
| or      | 405 004 4601          | TR 2SA608-F-SPA             | or      | 645 016 9809          | PLUG, 16P               |
| or      | 405 004 5103          | TR 2SA608-G-SPA             | CN497   | 645 033 7826          | PLUG, 11P               |
| or      | 405 006 1806          | TR 2SA933S-R                | D1101   | 407 221 1807          | DIODE KDS120E           |
| or      | 405 006 1905          | TR 2SA933S-S                | or      | 407 179 1805          | DIODE DAP222            |
| Q4006   | $\Delta$ 405 138 6502 | TR KTB1366Y                 | D1102   | 407 221 1906          | DIODE KDS121E           |
| Q4007   | 405 143 6504          | TR KTA1267-GR               | or      | 407 162 8507          | DIODE DAN222            |
| or      | 405 004 4601          | TR 2SA608-F-SPA             | D4100   | $\Delta$ 407 196 5800 | DIODE 1N5402BD82        |
| or      | 405 004 5103          | TR 2SA608-G-SPA             | D4101   | $\Delta$ 407 196 5800 | DIODE 1N5402BD82        |
| or      | 405 006 1806          | TR 2SA933S-R                | D4102   | $\Delta$ 407 196 5800 | DIODE 1N5402BD82        |
| or      | 405 006 1905          | TR 2SA933S-S                | D4103   | $\Delta$ 407 196 5800 | DIODE 1N5402BD82        |
| R4008   | $\Delta$ 402 081 1004 | FUSIBLE RES 10 JA 1/4W      | D4104   | $\Delta$ 407 196 5800 | DIODE 1N5402BD82        |
| R4013   | $\Delta$ 402 083 7707 | RESISTOR 1K J-1W            | D4105   | $\Delta$ 407 196 5800 | DIODE 1N5402BD82        |
| WR401   | 614 017 8203          | TERMINAL BOARD              | D4106   | $\Delta$ 407 097 8009 | DIODE MPG06G            |
| WR402   | 614 017 8203          | TERMINAL BOARD              | D4107   | $\Delta$ 407 097 8009 | DIODE MPG06G            |

### MAIN, AMP/DVD P.W.BAORD ASSY

| REF.NO. | PART NO.              | DESCRIPTION               | REF.NO. | PART NO.              | DESCRIPTION           |
|---------|-----------------------|---------------------------|---------|-----------------------|-----------------------|
| 73      | 614 324 0617          | ASSY, PWB, MAIN, AMP, DVD | D4111   | $\Delta$ 407 097 8009 | DIODE MPG06G          |
|         |                       | (Only initial)            | D4112   | 407 099 5303          | ZENER DIODE MTZJ5.6B  |
| C1050   | $\Delta$ 403 373 7902 | ELECT 150U M 6.3V         | D4113   | 407 099 5303          | ZENER DIODE MTZJ30B   |
| C1901   | $\Delta$ 403 373 7902 | ELECT 150U M 6.3V         | D4114   | $\Delta$ 408 044 6307 | DIODE SB140L 19C2-004 |
| C4102   | 403 325 0302          | ELECT 2200U M 25V         | D4115   | $\Delta$ 408 044 6307 | DIODE SB140L 19C2-004 |
|         |                       |                           | D4199   | $\Delta$ 407 099 5303 | ZENER DIODE MTZJ5.6B  |



DM01

DM02

DM03

DM04

DM05

DM06

DM07

DM08

DM09

DM10

DM11

DM12

DM13

DM14

DM17

DM18

DM19

DM20

DM21

DM22

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DM24

DM25

DM26

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DM28

DM29

DM30

DM32

DM33

DM34

DM36

DM37

DM38

DM39

## DVD MECHANISM ASSY

| REF.NO. | PART NO.     | DESCRIPTION                               |
|---------|--------------|-------------------------------------------|
|         | 614 324 6954 | ASSY,MECHA,KIT770AVM2                     |
| DM02    | 614 320 2264 | DISC,CHUCK DISC                           |
| DM03    | 614 320 2356 | SLIDE,BASE UP/DOWN                        |
| DM04    | 614 323 3963 | BELT,SQUARE,LOADING                       |
| DM05    | 614 320 2271 | GEAR,LOADING GEAR                         |
| DM06    | 412 061 7803 | SPECIAL SCREW,HOLDER RAIL FIX             |
| DM07    | 614 320 2349 | PULLEY,LOADING RETARD PULLY               |
| DM08    | 614 320 5845 | CHASSIS,LOADING CHASSIS                   |
| DM09    | 614 320 2363 | TRAY,TRAY                                 |
| DM11    | 411 021 2704 | SCR S-TPG BIN 2.6X6,<br>PWB MECHA IF FIX  |
| DM12    | 645 032 4352 | ASSY,MOTOR,LOADING                        |
| DM13    | 645 051 4920 | MAGNET(CHUCK),MAGNET CHUCK                |
| DM14    | 614 320 2288 | HOLDER,CHUCK HOLDER                       |
| DM17    | 411 021 1806 | SCR S-TPG BIN 2.6X10,BASE FIX             |
| DM18    | 411 092 0906 | WASHER Z 2.6X10X0.5,BASE FIX              |
| DM19    | 614 324 6961 | ASSY, MECHA,<br>KIT700AVM2BASE,BASE MECHA |
| DM20    | 411 184 0302 | SCR S-TPG PAN PCS 1.7X4.5,<br>RACK FIX    |
| DM21    | 614 310 2083 | GEAR,RACK,MOVE PICKUP(FREE)               |
| DM22    | 614 310 6159 | SPRING,COMP,<br>FOR BACK RUSH(RACK)       |
| DM23    | 614 310 2076 | GEAR,RACK,MOVE PICKUP(FIX)                |
| DM24    | 411 018 4704 | SCR PAN PCS 1.7X5,LIMIT SW FIX            |
| DM25    | 645 040 9899 | SWITCH,MICRO 1P-2T,LIMIT SW               |
| DM26    | 412 057 8304 | SPECIAL WASHER,FOR GEAR 4 FIX             |
| DM27    | 614 310 2069 | GEAR,GEAR-5                               |
| DM28    | 614 310 6142 | SPRING,COMP,FOR BACK RUSH                 |
| DM29    | 614 310 2052 | GEAR,,GEAR-4                              |
| DM30    | 412 057 8304 | SPECIAL WASHER,FOR GEAR 2 FIX             |
| DM32    | 614 310 2038 | GEAR,,GEAR-2                              |
| DM33    | 411 106 7709 | SCR PAN PCS 1.7X2.5,<br>SLED MOTOR FIX    |
| DM34    | 645 051 5194 | ASSY,MOTOR,SLED MOTOR                     |
| DM36    | 614 310 2045 | GEAR,,GEAR-3                              |
| DM37    | 614 320 2301 | MOUNTING,<br>BASE MECHA MOUNTING          |
| DM38    | 614 310 6128 | SPACER,MECHA,<br>BASE MECHA FLOATING      |

| REF.NO. | PART NO.     | DESCRIPTION                          |
|---------|--------------|--------------------------------------|
| DM39    | 614 322 9070 | SPACER,MECHA,<br>BASE MECHA FLOATING |

| MECHA SW P.W.BOARD ASSY |              |                                 |
|-------------------------|--------------|---------------------------------|
| REF.NO.                 | PART NO.     | DESCRIPTION                     |
| DM10                    | 614 320 2219 | ASSY,PWB MECHA SW(Only initial) |
| CN001                   | 645 006 0922 | PLUG,5P,MOTOR & SW PLUG         |
| or                      | 614 310 2618 | PLUG,5P,MOTOR & SW PLUG         |
| S0001                   | 645 051 5378 | SWITCH,LEVER,MECHA SW           |

| MECHA SW P.W.BOARD ASSY |              |                                 |
|-------------------------|--------------|---------------------------------|
| REF.NO.                 | PART NO.     | DESCRIPTION                     |
| DM10                    | 614 320 2219 | ASSY,PWB MECHA SW(Only initial) |
| CN001                   | 645 006 0922 | PLUG,5P,MOTOR & SW PLUG         |
| or                      | 614 310 2618 | PLUG,5P,MOTOR & SW PLUG         |
| S0001                   | 645 051 5378 | SWITCH,LEVER,MECHA SW           |

| REF. NO. | PART NO.       | DESCRIPTION                   |
|----------|----------------|-------------------------------|
| X4300    | 645 033 4393   | OSC.CERAMIC 8.00MHZ           |
| X4301    | 645 053 8339   | OSC.CRYSTAL 32.768KHZ         |
| X8000    | 645 032 1627   | OSC.CRYSTAL 32.768KHZ         |
| X8000    | 645 052 2994   | OSC.CERAMIC 12.50MHZ          |
| X8230    | 645 045 8293   | OSC.CRYSTAL 27.000MHZ         |
| 74       | 614 321 8296   | ASSY,PWB,HEADPHONE/MIC        |
| REF. NO. | PART NO.       | DESCRIPTION                   |
| CN405    | 614 310 2519   | PLUG,10P                      |
| CN406    | 645 005 009    | PLUG,10P                      |
| CN407    | 645 009 0042   | JACK,PHONE DE 43              |
| L4050    | 645 001 4550   | INDUCTOR,100U K               |
| L4070    | 645 001 4550   | INDUCTOR,100U K               |
| Q4070    | 645 143 8706   | TR KT031799-GR                |
| or       | 645 017 9600   | TR 2SC3330-T                  |
| or       | 405 017 9709   | TR 2SC3330-U                  |
| or       | 405 011 8500   | TR 2SC1740S-R                 |
| or       | 405 011 8609   | TR 2SC1740S-S                 |
| R4050    | Δ 402 082 1201 | RESISTOR 330 U - 1W           |
| R4051    | Δ 402 082 1201 | RESISTOR 330 U - 1W           |
| SC405    | 645 045 7449   | SURGE-ABSORBER                |
| SC406    | 645 045 7449   | SURGE-ABSORBER                |
| SC407    | 645 045 7449   | SURGE-ABSORBER                |
| SG408    | 645 045 7449   | SURGE-ABSORBER                |
| 75       | 614 324 0631   | ASSY,PWB,TUNNER(Only Initial) |
| REF. NO. | PART NO.       | DESCRIPTION                   |
| CN201    | 645 005 0695   | TERMINAL,ANT                  |
| CN202    | 645 031 7910   | TERMINAL                      |
| CN241    | 614 221 8273   | SOCKET,11P                    |
| CN241    | 645 033 7833   | SOCKET,11P                    |
| D2101    | 407 157 8109   | VARACTOR DI SV2C11-B          |
| D2102    | 407 157 8109   | VARACTOR DI SV2C11-B          |
| D2103    | 407 012 4406   | DIODE 1SS133                  |
| D2104    | 407 012 4406   | DIODE 1SS133                  |
| D2105    | 407 012 4406   | DIODE 1SS133                  |
| D2301    | 407 063 9108   | ZENER DIODE MTJ26-8B          |
| D2451    | 407 012 4406   | DIODE 1SS133                  |
| D2452    | 407 153 7502   | ZENER DIODE GZS3-0B           |
| D2454    | 407 012 4406   | DIODE 1SS133                  |
| IC211    | 409 292 5807   | IC T81768SN                   |
| IC231    | 409 474 3201   | IC L81442ML                   |
| IC241    | 409 439 4502   | IC LC72121M-D                 |
| L2101    | 645 018 0163   | COIL,AIR                      |
| L2102    | 645 018 0255   | COIL,AIR                      |
| L2151    | 645 002 1534   | INDUCTOR,8.2U K               |
| L2451    | 645 003 1789   | INDUCTOR,8.2U K               |
| L2451    | 645 001 4581   | TUNER                         |
| L2503    | 645 003 17842  | INDUCTOR,100U K               |
| Q2451    | 405 000 0904   | TR D7A114VS                   |
| R2101    | Δ 401 017 0708 | CARBON 270 JA 1/4W            |
| R2301    | Δ 401 017 0708 | CARBON 270 JA 1/4W            |
| R2451    | Δ 401 017 0708 | CARBON 270 JA 1/4W            |
| XF211    | 645 026 2975   | FLTER,BP 108MHZ               |
| XF221    | 645 012 1045   | FLTER,LC                      |
| or       | 645 010 7665   | CERAMIC FLTER 10.70MHZ        |
| or       | 614 221 0199   | FLTER                         |
| or       | 614 030 5074   | FLTER                         |
| or       | 645 010 7665   | CERAMIC FLTER 10.70MHZ        |
| or       | 614 221 0199   | FLTER                         |
| or       | 614 030 5074   | FLTER                         |
| XF231    | 614 246 0849   | FLTER                         |
| XF233    | 645 039 9923   | TRANS,IF 10.7MHZ              |

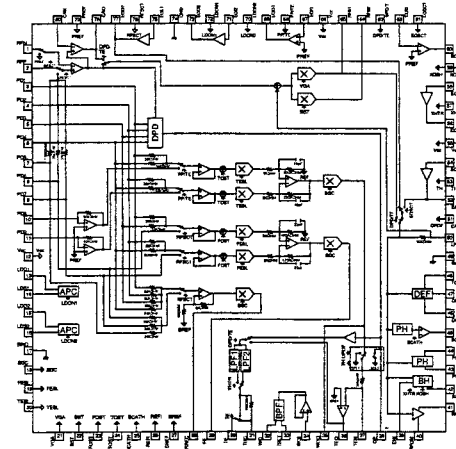
| PART NO.     | DESCRIPTION             | REF. NO. |
|--------------|-------------------------|----------|
| 405 141 5608 | TR DTC1414YKA           | Q4621    |
| 405 141 5608 | TR KRC107S              | Q4640    |
| 405 166 7007 | TR KTD1304              | Q4641    |
| 405 166 7007 | TR KTD1304              | Q4741    |
| 405 166 7007 | TR KTD1304              | Q4840    |
| 405 166 7007 | TR KTD1304              | Q4841    |
| 405 151 6107 | TR KRA107S              | Q4842    |
| 405 141 5608 | TR DTA114YKA            | Q4843    |
| 405 151 6107 | TR KRC107S              | Q4844    |
| 405 141 5608 | TR DTC1414YKA           | Q4845    |
| 405 151 6107 | TR KRA107S              | Q4846    |
| 405 159 0503 | TR DTA114YKA            | Q4847    |
| 405 141 5608 | TR DTC1414YKA           | Q4848    |
| 405 141 5608 | TR KRC107S              | Q4849    |
| 405 151 6107 | TR KRA107S              | Q4900    |
| 405 166 7007 | TR DTA114YKA            | Q4901    |
| 405 166 7007 | TR KTD1304              | Q4902    |
| 405 159 0503 | TR KRC107S              | Q4903    |
| 405 141 5608 | TR DTC1414YKA           | Q4920    |
| 405 151 6107 | TR KRA107S              | Q4921    |
| 405 141 5608 | TR DTA114YKA            | Q4980    |
| 405 146 1704 | TR KTA1504-Y            | Q49880   |
| 405 146 1704 | TR KTA1504-Y            | or       |
| 405 124 5905 | TR KTA1504-GH           | or       |
| 405 103 0308 | TR DSA1037K-R           | or       |
| 405 005 5508 | TR DSA812-M6            | or       |
| 405 199 0503 | TR KRC107S              | Q49882   |
| 405 141 5608 | TR DTC1414YKA           | or       |
| 405 202 8205 | MT-GLAZE 3K FA 1/16W    | RA1107   |
| 401 220 2503 | MT-GLAZE 3K FA 1/16W    | RA1108   |
| 401 218 4604 | MT-GLAZE 5.6K FA 1/16W  | RA1112   |
| 401 230 2503 | MT-GLAZE 1K FA 1/16W    | RA1115   |
| 402 081 0106 | FUSIBLE RES 2.2 JA 1/4W | RA1116   |
| 402 085 2205 | RESISTOR 6.8 J 2W       | RA1115   |
| 402 082 1300 | RESISTOR 4.7 J 1W       | RA1111   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1109   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1108   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1107   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1106   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1105   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1104   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1103   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1102   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1101   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1100   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1099   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1098   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1097   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1096   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1095   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1094   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1093   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1092   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1091   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1090   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1089   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1088   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1087   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1086   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1085   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1084   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1083   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1082   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1081   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1080   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1079   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1078   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1077   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1076   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1075   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1074   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1073   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1072   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1071   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1070   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1069   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1068   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1067   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1066   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1065   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1064   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1063   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1062   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1061   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1060   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1059   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1058   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1057   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1056   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1055   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1054   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1053   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1052   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1051   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1050   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1049   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1048   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1047   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1046   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1045   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1044   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1043   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1042   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1041   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1040   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1039   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1038   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1037   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1036   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1035   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1034   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1033   |
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| 402 082 2802 | RESISTOR 10 J 1W        | RA1031   |
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| 402 082 2802 | RESISTOR 10 J 1W        | RA1029   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1028   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1027   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1026   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1025   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1024   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1023   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1022   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1021   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1020   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1019   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1018   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1017   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1016   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1015   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1014   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1013   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1012   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1011   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1010   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1009   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1008   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1007   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1006   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1005   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1004   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1003   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1002   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1001   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA1000   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA0999   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA0998   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA0997   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA0996   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA0995   |
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| 402 082 2802 | RESISTOR 10 J 1W        | RA0960   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA0959   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA0958   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA0957   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA0956   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA0955   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA0954   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA0953   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA0952   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA0951   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA0950   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA0949   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA0948   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA0947   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA0946   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA0945   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA0944   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA0943   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA0942   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA0941   |
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| 402 082 2802 | RESISTOR 10 J 1W        | RA0938   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA0937   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA0936   |
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| 402 082 2802 | RESISTOR 10 J 1W        | RA0925   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA0924   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA0923   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA0922   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA0921   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA0920   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA0919   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA0918   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA0917   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA0916   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA0915   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA0914   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA0913   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA0912   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA0911   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA0910   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA0909   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA0908   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA0907   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA0906   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA0905   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA0904   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA0903   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA0902   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA0901   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA0900   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA0899   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA0898   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA0897   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA0896   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA0895   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA0894   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA0893   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA0892   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA0891   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA0890   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA0889   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA0888   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA0887   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA0886   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA0885   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA0884   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA0883   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA0882   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA0881   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA0880   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA0879   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA0878   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA0877   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA0876   |
| 402 082 2802 | RESISTOR 10 J 1W        | RA0875   |

## IC BLOCK DIAGRAM & DESCRIPTION

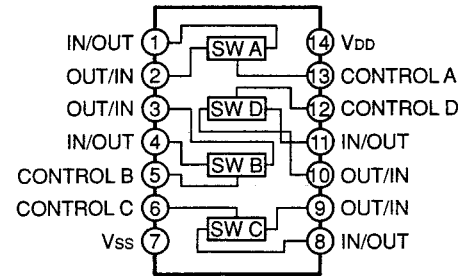
### IC100 LA9702WL-MPB (Read Channel)

| Pin No. | Pin name | Function                                                         |
|---------|----------|------------------------------------------------------------------|
| 1       | RFN      | RF signal - input                                                |
| 2       | RFP      | RF signal + input                                                |
| 3       | PD1      | Pickup signal input                                              |
| 4       | PD2      | Pickup signal input                                              |
| 5       | PD3      | Pickup signal input                                              |
| 6       | PD4      | Pickup signal input                                              |
| 7       | PD5      | Pickup signal input                                              |
| 8       | PD6      | Pickup signal input                                              |
| 9       | PD7      | Pickup signal input                                              |
| 10      | PD8      | Pickup signal input                                              |
| 11      | PD9      | Pickup signal input                                              |
| 12      | VCC      | Power supply                                                     |
| 13      | LDD1     | APC1 output                                                      |
| 14      | LDS1     | APC1 monitor power input                                         |
| 15      | LDD2     | APC2 output                                                      |
| 16      | LDS2     | APC2 monitor power input                                         |
| 17      | GND      | GND                                                              |
| 18      | SGC      | Servo gain control terminal (RREC, FE, TE)                       |
| 19      | FEBL     | Focus balance adjustment terminal                                |
| 20      | TEBL     | Tracking balance adjustment terminal                             |
| 21      | VGA      | RF gain adjustment terminal                                      |
| 22      | BST      | Equalizer boost adjustment                                       |
| 23      | FOST     | Focus offset adjustment terminal                                 |
| 24      | TOST     | Tracking offset adjustment terminal                              |
| 25      | BCATH    | BCA shurehshud adjustment terminal                               |
| 26      | REF1     | Base power setting                                               |
| 27      | SREF     | Servo signal base power output                                   |
| 28      | RREC     | Reflection output                                                |
| 29      | FE       | Focus error output                                               |
| 30      | TE       | Tracking error output                                            |
| 31      | THC      | TE hold time constant value condenser connect                    |
| 32      | WO       | Wobble output terminal                                           |
| 33      | ISCT     | BPF center frequency setting register connect terminal           |
| 34      | WO1      | Push pull signal input                                           |
| 35      | WOO      | Push pull signal output                                          |
| 36      | TEO      | 3 beam TE gain setting terminal                                  |
| 37      | TEN      | 3 beam TE gain setting terminal                                  |
| 38      | CP       | Charge pump gain setting register, condenser connect terminal    |
| 39      | BHI      | Bottom hold detect constant setting register connection terminal |
| 40      | RFON     | RF - output                                                      |
| 41      | RFOP     | RF + output                                                      |
| 42      | BH       | RF bottom detection output                                       |
| 43      | PHI      | peak hold detection constant register connect                    |
| 44      | PH       | RF peak detection output                                         |
| 45      | BCA      | BCA output                                                       |

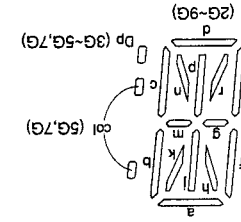
| Pin No. | Pin name | Function                                                  |
|---------|----------|-----------------------------------------------------------|
| 46      | DEF      | Defect output (H : Defect detection)                      |
| 47      | DEFC     | Defect detection condenser connect terminal               |
| 48      | TC       | Defect detection constant setting register terminal       |
| 49      | GND      | GND (D7D system)                                          |
| 50      | LPC      | RF DC servo condenser connect terminal                    |
| 51      | CPOF     | Charge pump OFF terminal (H : OFF)                        |
| 52      | EQO2     | RF equalizer setting terminal                             |
| 53      | TH       | Tracking hold (H : hold)                                  |
| 54      | EQL2     | RF equalizer setting terminal                             |
| 55      | VCC      | Power supply (DPD system)                                 |
| 56      | EQO4     | RF equalizer setting terminal                             |
| 57      | XHTR     | Tracking, bottom detection band switching (L : high band) |
| 58      | EQL4     | RF equalizer setting terminal                             |
| 59      | XQBH     | Bottom detection time constant switching (L : high speed) |
| 60      | EQO3     | RF equalizer setting terminal                             |
| 61      | EQSCT    | Equalizer switching (H : 77 pin select, L : 52pin select) |
| 62      | EQL3     | RF equalizer setting terminal                             |
| 63      | DPD/TE   | DPD, 3 beam tracking switching (H : DPD)                  |
| 64      | RFO2     | RF output                                                 |
| 65      | RFO1     | RF output                                                 |
| 66      | VCC      | Power supply (RF system)                                  |
| 67      | EQO1     | RF equalizer setting terminal                             |
| 68      | PP/TE    | 3 beam, push pull tracking switching (L : 3 beam)         |
| 69      | EQO1     | RF equalizer setting terminal                             |
| 70      | LDO2     | APC 2 beam laser ON terminal (H : ON)                     |
| 71      | EQL2     | RF equalizer setting terminal                             |
| 72      | LDO1     | APC 1 beam laser ON terminal (H : ON)                     |
| 73      | EQO2     | RF equalizer setting terminal                             |
| 74      | GND      | GND (RF system)                                           |
| 75      | EQL1     | RF equalizer setting terminal                             |
| 76      | RFSCCT   | RF input switching (H : RF differential input, PP error)  |
| 77      | EQO1     | RF equalizer setting terminal                             |
| 78      | CAO      | customize amp. output                                     |
| 79      | PREF     | Base voltage output (pick use)                            |
| 80      | CAN      | customize amp. input                                      |



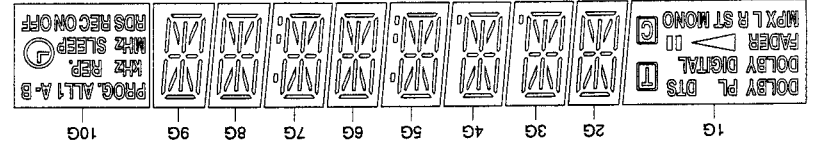
### IC101,493 CD40668BCM(Quad Bilateral Switch)



|       |    |    |    |     |    |     |    |    |    |      |     |
|-------|----|----|----|-----|----|-----|----|----|----|------|-----|
| -     | -  | -  | -  | Dp  | -  | Dp  | Dp | Dp | -  | -    | P16 |
| -     | -  | -  | -  | col | -  | col | -  | -  | -  | -    | P15 |
| OFF   | d  | d  | d  | d   | d  | d   | d  | d  | d  | -    | P14 |
| ON    | e  | e  | e  | e   | e  | e   | e  | e  | e  | MONO | P13 |
| SLEEP | u  | u  | u  | u   | u  | u   | u  | u  | u  | MONO | P12 |
| REC   | p  | p  | p  | p   | p  | p   | p  | p  | p  | MONO | P11 |
| REC   | r  | r  | r  | r   | r  | r   | r  | r  | r  | MONO | P10 |
| REC   | c  | c  | c  | c   | c  | c   | c  | c  | c  | MONO | P9  |
| REC   | m  | m  | m  | m   | m  | m   | m  | m  | m  | MONO | P8  |
| REC   | g  | g  | g  | g   | g  | g   | g  | g  | g  | MONO | P7  |
| REC   | f  | f  | f  | f   | f  | f   | f  | f  | f  | MONO | P6  |
| B     | k  | k  | k  | k   | k  | k   | k  | k  | k  | MONO | P5  |
| A     | j  | j  | j  | j   | j  | j   | j  | j  | j  | MONO | P4  |
| 1     | h  | h  | h  | h   | h  | h   | h  | h  | h  | MONO | P3  |
| ALT   | b  | b  | b  | b   | b  | b   | b  | b  | b  | MONO | P2  |
| PROG  | a  | a  | a  | a   | a  | a   | a  | a  | a  | MONO | P1  |
| 10G   | 9G | 8G | 7G | 6G  | 5G | 4G  | 3G | 2G | 1G | MONO | P1  |

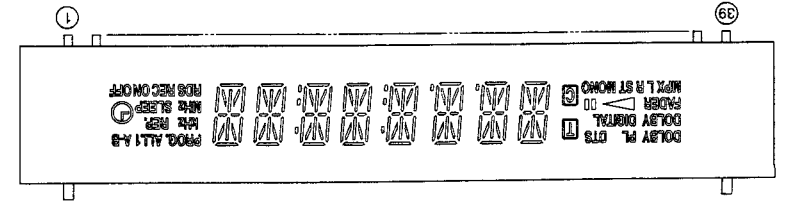


ANODE CONNECTION



| PIN NO.    | 1  | 2  | 3  | 4  | 5  | 6  | 7  | 8  | 9  | 10  | 11  | 12  | 13  | 14  | 15  | 16  | 17  | 18  | 19  | 20  | 21  | 22  | 23  | 24  | 25  | 26  | 27  | 28  | 29  | 30  | 31  | 32  | 33  | 34  | 35  | 36  | 37  | 38  | 39  |
|------------|----|----|----|----|----|----|----|----|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| CONNECTION | F1 | F2 | F3 | F4 | F5 | F6 | F7 | F8 | F9 | F10 | F11 | F12 | F13 | F14 | F15 | F16 | F17 | F18 | F19 | F20 | F21 | F22 | F23 | F24 | F25 | F26 | F27 | F28 | F29 | F30 | F31 | F32 | F33 | F34 | F35 | F36 | F37 | F38 | F39 |

PIN CONNECTION



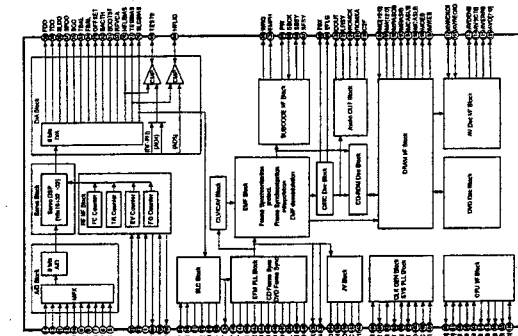
FL601 Fluorescent Tube

## IC BLOCK DIAGRAM & DESCRIPTION

# IC BLOCK DIAGRAM & DESCRIPTION IC130 LC78661W-D(DVD/CD Signal Processing)

| Block        | Pin # | Pin Name | IO | Supplementation                                                               |
|--------------|-------|----------|----|-------------------------------------------------------------------------------|
| AV data IF   | 111   | AVREQO   | IO | AV data demand flag I/O pins                                                  |
|              | 112   | AVACKO   | IO | AV data read strobe output pin                                                |
|              | 113   | AVDACK   | IO | AV data read (Clock/Enable) output pins                                       |
|              | 114   | AVSCTB   | O  | AV output sector synchronization output pin                                   |
|              | 115   | AVERRB   | O  | AV data release flag output pin                                               |
| Power supply | 116   | DVSS     | -  | Digital GND                                                                   |
|              | 117   | DVDD4    | -  | VO power supply (Digital 3.3V or 5V) [106 to 136]                             |
|              | 118   | AVDQ     | O  | AV data 0                                                                     |
|              | 119   | AVD1     | O  | AV data 1                                                                     |
|              | 120   | AVD2     | O  | AV data 2                                                                     |
| AV data IF   | 121   | AVD3     | O  | AV data 3                                                                     |
|              | 122   | AVD4     | O  | AV data 4                                                                     |
|              | 123   | AVD5     | O  | AV data 5                                                                     |
|              | 124   | AVD6     | O  | AV data 6                                                                     |
|              | 125   | AVD7     | O  | AV data 7                                                                     |
| CD data      | 126   | CDP      | O  | CD flag output pin                                                            |
|              | 127   | ROMAXA   | O  | CD data output pin                                                            |
|              | 128   | ROMCK    | O  | CD data output shift lock output pin                                          |
|              | 129   | LRBY     | O  | CD data output L/R clock output pin                                           |
|              | 130   | EMPH     | O  | Overmode monitor pin                                                          |
| Digital OUT  | 131   | DOCT     | O  | Audio SIA data output pin                                                     |
|              | 132   | DVDD4    | VO | VO power supply (Digital 3.3V or 5V) [106 to 136]                             |
|              | 133   | DVSS     | -  | Digital GND                                                                   |
|              | 134   | EFMOUT   | O  | EFM 2 value signal output pin                                                 |
|              | 135   | LEFM     | O  | Output pin for the signal picked out from EFM binary signal with PCK          |
| Power supply | 136   | PCK      | O  | EFM playback shift clock output pin                                           |
|              | 137   | DVDD0    | -  | Inner logic power supply (Digital 3.3V)                                       |
|              | 138   | DVSS     | -  | Digital GND                                                                   |
|              | 139   | VCOCTL   | VO | VCO filter connection pin                                                     |
|              | 140   | PPDO     | -  | Phase comparison filter connection pin                                        |
| EFM PLL      | 141   | PPDO     | -  | Frequency comparison filter connection pin                                    |
|              | 142   | LF1      | -  | Filter connection pin 1                                                       |
|              | 143   | LF2      | -  | Filter connection pin 2                                                       |
|              | 144   | LF3      | -  | Filter connection pin 3                                                       |
|              | 145   | PCN      | -  | Voltage monitor pin (Phase comparison charge pump PCH control voltage)        |
| Power supply | 146   | FISET    | -  | Current setting pin for the constant-current phase comparison charge pump     |
|              | 147   | FISET    | -  | Current setting pin for the constant-current frequency comparison charge pump |
|              | 148   | QDPR     | -  | EFM playback VCO oscillator range setting pin (F or CD)                       |
|              | 149   | QDPR     | -  | EFM playback VCO oscillator range setting pin (F or DVD)                      |
|              | 150   | AVDD2    | -  | EFM PLL JV power supply (Analog 5V)                                           |
| JV           | 151   | AVSS     | -  | Analog GND                                                                    |
|              | 152   | JVCP1    | -  | JV control pin                                                                |
|              | 153   | JVCP2    | -  | JV control pin                                                                |
|              | 154   | JVAC     | -  | EFM playback PLL clock filter output pin                                      |
|              | 155   | JVAIN    | -  | JV control pin                                                                |
| Power supply | 156   | JVRYO    | -  | JV control pin                                                                |
|              | 157   | AVDD4    | -  | SYSTEM PLL power supply (Analog 3.3V)                                         |
|              | 158   | AVSS     | -  | Analog GND                                                                    |
|              | 159   | MD15     | IO | DRAM data 15                                                                  |
|              | 160   | MD14     | IO | DRAM data 14                                                                  |
| DRAM IF      | 161   | MD13     | IO | DRAM data 13                                                                  |
|              | 162   | MD12     | IO | DRAM data 12                                                                  |
|              | 163   | MD11     | IO | DRAM data 11                                                                  |
|              | 164   | MD10     | IO | DRAM data 10                                                                  |
|              | 165   | MD9      | IO | DRAM data 9                                                                   |
| Power supply | 166   | MD8      | IO | DRAM data 8                                                                   |
|              | 167   | DVDD5    | -  | VO power supply (Digital 3.3V or 5V) [159 to 197]                             |
|              | 168   | DVSS     | -  | Digital GND                                                                   |
|              | 169   | MD7      | IO | DRAM data 7                                                                   |
|              | 170   | MD6      | IO | DRAM data 6                                                                   |
| DRAM IF      | 171   | MD5      | IO | DRAM data 5                                                                   |
|              | 172   | MD4      | IO | DRAM data 4                                                                   |
|              | 173   | MD3      | IO | DRAM data 3                                                                   |
|              | 174   | MD2      | IO | DRAM data 2                                                                   |
|              | 175   | MD1      | IO | DRAM data 1                                                                   |
| Power supply | 176   | MD0      | IO | DRAM data 0                                                                   |
|              | 177   | MA0      | O  | DRAM address 0                                                                |
|              | 178   | MA1      | O  | DRAM address 1                                                                |
|              | 179   | MA2      | O  | DRAM address 2                                                                |
|              | 180   | MA3      | O  | DRAM address 3                                                                |
| DRAM IF      | 181   | MA4      | O  | DRAM address 4                                                                |
|              | 182   | MA5      | O  | DRAM address 5                                                                |
|              | 183   | MA6      | O  | DRAM address 6                                                                |
|              | 184   | MA7      | O  | DRAM address 7                                                                |
|              | 185   | DVDD5    | -  | VO power supply (Digital 3.3V or 5V) [159 to 197]                             |
| Power supply | 186   | DVSS     | -  | Digital GND                                                                   |
|              | 187   | MA8      | O  | DRAM address 8                                                                |
|              | 188   | MA9      | O  | DRAM address 9                                                                |
|              | 189   | MA10     | O  | DRAM address 10                                                               |
|              | 190   | MA11     | O  | DRAM address 11                                                               |
| DRAM IF      | 191   | MA12     | O  | DRAM address 12                                                               |
|              | 192   | MRAS0B   | O  | RAS output pin 0                                                              |
|              | 193   | MRAS1B   | O  | RAS output pin 1                                                              |
|              | 194   | MCASUB   | O  | CAS output pin (Upper Byte)                                                   |
|              | 195   | MCASLB   | O  | CAS output pin (Lower Byte)                                                   |
| Power supply | 196   | MCER     | O  | OE output pin                                                                 |
|              | 197   | MWES     | O  | WE output pin                                                                 |
|              | 198   | DVSS     | -  | Digital GND                                                                   |
|              | 199   | DVDD0    | -  | Inner logic power supply (Digital 3.3V)                                       |
|              | 200   | RFP0     | O  | RF general-purpose port output pin 0                                          |
| Power supply | 201   | RFP1     | O  | RF general-purpose port output pin 1                                          |
|              | 202   | RFP2     | O  | RF general-purpose port output pin 2                                          |
|              | 203   | RFP3     | O  | RF general-purpose port output pin 3                                          |
|              | 204   | RFP4     | O  | RF general-purpose port output pin 4                                          |
|              | 205   | DEFECTO  | O  | Defect signal output pin                                                      |
| Power supply | 206   | DEFECT1  | O  | Defect signal output pin                                                      |
|              | 207   | DVSS     | -  | Digital GND                                                                   |
|              | 208   | DVDD1    | -  | VO power supply (Digital 3.3V or 5V) [1 to 2, 200 to 208]                     |

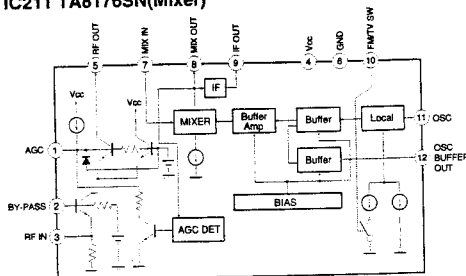
# IC BLOCK DIAGRAM & DESCRIPTION IC130 LC78661W-D(DVD/CD Signal Processing)



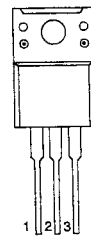
| Block        | Pin # | Pin Name | IO | Supplementation                                              |
|--------------|-------|----------|----|--------------------------------------------------------------|
| RF IF        | 1     | RFP1     | O  | RF input port pin                                            |
|              | 2     | TERBO    | IO | Tracking margin signal I/O pin                               |
| Power supply | 3     | DVDD2    | -  | AVD D/A internal logic power supply (Digital 5V)             |
|              | 4     | DVSS     | -  | Digital GND                                                  |
| AD           | 5     | AD0      | I  | Servo A/D input pin (AD0: Assistant input 0)                 |
|              | 6     | AD1      | I  | Servo A/D input pin (AD1: Assistant input 1)                 |
|              | 7     | AD2      | I  | Servo A/D input pin (AD2: Assistant input 2)                 |
|              | 8     | AD3      | I  | Servo A/D input pin (AD3: Assistant input 3)                 |
|              | 9     | AD4      | I  | Servo A/D input pin (AD4: Assistant input 4)                 |
|              | 10    | AD5      | I  | Servo A/D input pin (AD5: Assistant input 5)                 |
|              | 11    | RF_P1    | I  | Servo A/D input pin (RF_P1: RF peak hold signal)             |
|              | 12    | RF_P2    | I  | Servo A/D input pin (RF_P2: RF peak hold signal)             |
|              | 13    | TE       | I  | Servo A/D input pin (TE: Tracking error signal)              |
|              | 14    | FE       | I  | Servo A/D input pin (FE: Focus error signal)                 |
| TEST pin     | 15    | TEST0    | I  | Test input pin 0 (L, Fixed)                                  |
|              | 16    | TEST1    | I  | Test input pin 1 (L, Fixed)                                  |
| S.C          | 17    | EFMAMP   | I  | EFMAMP input pin                                             |
|              | 18    | EFMAMP   | I  | EFMAMP input pin                                             |
|              | 19    | SLC_LPF0 | -  | SLC LFP pin                                                  |
|              | 20    | SLC_LPF1 | -  | SLC LFP pin                                                  |
|              | 21    | SLC_LPF2 | -  | SLC LFP pin                                                  |
|              | 22    | SLC_LPF3 | -  | SLC LFP pin                                                  |
|              | 23    | SLC_LPF4 | -  | SLC LFP pin                                                  |
|              | 24    | SLC_LPF5 | -  | SLC LFP pin                                                  |
|              | 25    | SLC_LPF6 | -  | SLC LFP pin                                                  |
|              | 26    | SLC_LPF7 | -  | SLC LFP pin                                                  |
| Power supply | 27    | AVDD1    | -  | AVD D/A SLC power supply (Analog 5V)                         |
|              | 28    | AVSS     | -  | Analog GND                                                   |
|              | 29    | VREF     | O  | Servo D/A standard voltage                                   |
|              | 30    | SLCBIAS  | O  | Servo D/A output pin (SLCBIAS: SLC standard voltage signal)  |
|              | 31    | TESBIAS  | O  | Servo D/A output pin (TESBIAS: TES standard voltage signal)  |
|              | 32    | HFLBIAS  | O  | Servo D/A output pin (HFLBIAS: HFL standard voltage signal)  |
|              | 33    | OFFBIAS  | O  | Servo D/A output pin (OFFBIAS: Assistant signal)             |
|              | 34    | SCATH    | O  | Servo D/A output pin (SCATH: Assistant signal)               |
|              | 35    | SCOTT3   | O  | Servo D/A output pin (SCOTT3: Assistant signal)              |
|              | 36    | RFVCA    | O  | Servo D/A output pin (RFVCA: Assistant signal)               |
| Power supply | 37    | TBAL     | O  | Servo D/A output pin (TBAL: Tracking balance control signal) |
|              | 38    | FBAL     | O  | Servo D/A output pin (FBAL: Focus balance control signal)    |
|              | 39    | SGC      | O  | Servo D/A output pin (SGC: Assistant signal)                 |
|              | 40    | SLDO     | O  | Servo D/A output pin (SLDO: Thread control signal)           |
|              | 41    | SPDO     | O  | Servo D/A output pin (SPDO: Spherule control signal)         |
|              | 42    | TDO      | O  | Servo D/A output pin (TDO: Tracking control signal)          |
|              | 43    | FOO      | O  | Servo D/A output pin (FOO: Focus control signal)             |
|              | 44    | DVSS     | -  | Digital GND                                                  |
|              | 45    | DVDD3    | -  | Internal logic power supply (Digital 3.3V)                   |
|              | 46    | PG       | I  | PG detector input pin                                        |
| RF IF        | 47    | EVENT    | I  | EVENT detector input pin                                     |
|              | 48    | HFLD     | IO | Mirror detector signal I/O pin                               |
|              | 49    | PP0      | IO | General-purpose port 0                                       |
|              | 50    | PP1      | IO | General-purpose port 1                                       |
|              | 51    | PP2      | IO | General-purpose port 2                                       |
|              | 52    | PP3      | IO | General-purpose port 3                                       |
|              | 53    | WFO      | O  | Subcode Q reset ready monitor pin                            |
|              | 54    | HFLBYD   | O  | DSF command decoder busy signal output pin                   |
|              | 55    | HFLBYD   | O  | DSF command decoder busy signal output pin                   |
|              | 56    | DVDD3    | -  | VO power supply (Digital 3.3V or 5V) [42 to 97]              |
| Power supply | 57    | DVSS     | -  | Digital GND                                                  |

| Block         | Pin # | Pin Name  | IO | Supplementation                                                 |
|---------------|-------|-----------|----|-----------------------------------------------------------------|
| VF            | 54    | HWATB     | O  | Wall signal output pin                                          |
|               | 55    | HR0B      | O  | Interrupt signal output pin                                     |
|               | 56    | DVDESB    | I  | Decoder reset input pin                                         |
|               | 57    | RESB      | I  | Servo reset input pin                                           |
|               | 58    | HR0B      | I  | Read signal input pin                                           |
|               | 59    | HWRB      | I  | Write signal input pin                                          |
|               | 60    | HCSB      | I  | Chip select signal input pin                                    |
|               | 61    | MDAT0     | IO | Data 0                                                          |
|               | 62    | MDAT1     | IO | Data 1                                                          |
|               | 63    | MDAT2     | IO | Data 2                                                          |
| Microcomputer | 64    | MDAT3     | IO | Data 3                                                          |
|               | 65    | MDAT4     | IO | Data 4                                                          |
|               | 66    | MDAT5     | IO | Data 5                                                          |
|               | 67    | MDAT6     | IO | Data 6                                                          |
|               | 68    | MDAT7     | IO | Data 7                                                          |
|               | 69    | HADR0     | I  | Address 0                                                       |
|               | 70    | HADR1     | I  | Address 1                                                       |
|               | 71    | HADR2     | I  | Address 2                                                       |
|               | 72    | HADR3     | I  | Address 3                                                       |
|               | 73    | HADR4     | I  | Address 4                                                       |
| IF            | 74    | HADR5     | I  | Address 5                                                       |
|               | 75    | HADR6     | I  | Address 6                                                       |
|               | 76    | HADR7     | I  | Address 7                                                       |
|               | 77    | HADR8     | I  | Address 8                                                       |
|               | 78    | HADR9     | I  | Address 9                                                       |
|               | 79    | HADR10    | I  | Address 10                                                      |
|               | 80    | HADR11    | I  | Address 11                                                      |
|               | 81    | HADR12    | I  | Address 12 (Buffer memory access selector pin (MCSEL))          |
|               | 82    | DVDD5     | -  | VO power supply (Digital 3.3V or 5V) [42 to 97]                 |
|               | 83    | DVSS      | -  | Digital GND                                                     |
| Subcode       | 84    | PW_AICND  | O  | Subcode (P,Q,R,S,T,U,V and W) data output pin / Monitor pin 0   |
|               | 85    | 88CK      | I  | Subcode block readout shift clock input pin                     |
|               | 86    | 88BY      | O  | Subcode block synchronization signal output pin                 |
|               | 87    | SPV_AICND | O  | Subcode frame synchronization signal output pin / Monitor pin 1 |
|               | 88    | SPV_AICND | O  | Subcode frame synchronization signal output pin / Monitor pin 2 |
|               | 89    | SPV_AICND | O  | Subcode frame synchronization signal output pin / Monitor pin 3 |
|               | 90    | SPV_AICND | O  | Subcode frame synchronization signal output pin / Monitor pin 4 |
|               | 91    | PP4       | IO | General-purpose port 4                                          |
|               | 92    | PP5       | IO | General-purpose port 5                                          |
|               | 93    | PP6       | IO | General-purpose port 6                                          |
| SYSTEM CLK    | 94    | X18MOUT   | O  | Internal 18MHz output pin                                       |
|               | 95    | X18M1N    | I  | External 18MHz input pin                                        |
|               | 96    | TEST2     | I  | Test input pin 2 (L, Fixed)                                     |
|               | 97    | DVDDCKOUT | O  | Internal DVD clock output pin                                   |
|               | 98    | DVDDCKIN  | I  | External DVD clock input pin                                    |
|               | 99    | TEST3     | I  | Test input pin 3 (L, Fixed)                                     |
|               | 100   | TEST4     | I  | Test input pin 4 (L, Fixed)                                     |
|               | 101   | TEST5     | I  | Test input pin 5 (L, Fixed)                                     |
|               | 102   | TEST6     | I  | Test input pin 6 (L, Fixed)                                     |
|               | 103   | TEST7     | I  | Test input pin 7 (L, Fixed)                                     |
| Power supply  | 104   | DVSS      | -  | Digital GND                                                     |
|               | 105   | DVDD4     | -  | VO power supply (Digital 3.3V)                                  |
|               | 106   | DVSS      | -  | Digital GND                                                     |
|               | 107   | XIN       | I  | Oscillator circuit input pin                                    |
|               | 108   | XOUT      | O  | Oscillator circuit output pin                                   |
|               | 109   | DVDD4     | -  | Oscillator circuit power supply (Digital 3.3V)                  |
|               | 110   | DVSS      | -  | Digital GND                                                     |
|               | 111   | PP7       | IO | General-purpose port 7                                          |
|               | 112   | PP8       | IO | General-purpose port 8                                          |
|               | 113   | PP9       | IO | General-purpose port 9                                          |

IC211 TA8176SN(Mixer)



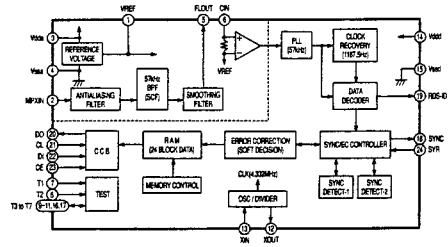
IC401 KIA7805AP(Regulator)



1. INPUT  
2. COMMON  
3. OUTPUT

## IC BLOCK DIAGRAM & DESCRIPTION

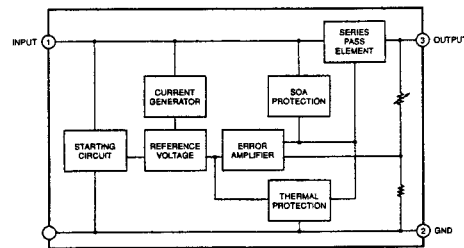
### IC251 LC72722(RDS Signal Processor)



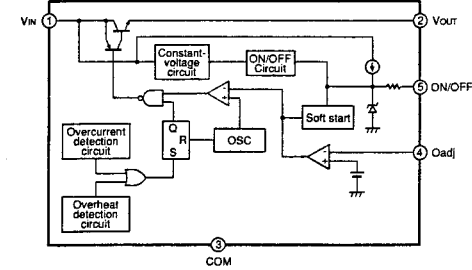
| Pin No. | Pin name                 | Function                                                                       | VO |
|---------|--------------------------|--------------------------------------------------------------------------------|----|
| 1       | VREF                     | Reference voltage output (V <sub>REF</sub> /2)                                 | O  |
| 2       | MPXIN                    | Baseband (multiplexed) signal input                                            | I  |
| 3       | FLOUT                    | Subcarrier output (filter output)                                              | O  |
| 4       | CIN                      | Subcarrier input (comparator input)                                            | I  |
| 5       | V <sub>SS</sub>          | Analog power supply (+5V)                                                      | -  |
| 6       | V <sub>SS</sub>          | Analog ground                                                                  | -  |
| 12      | XOUT                     | Crystal oscillator output (4.322/8.644MHz)                                     | O  |
| 13      | XIN                      | Crystal oscillator input (external reference signal input)                     | I  |
| 7       | T1                       | Test input (This pin must always be connected to ground.)                      | I  |
| 8       | T2                       | Test input (standby control)                                                   | I  |
| 9       | T3 (RDCL)                | 1-standby state (crystal oscillator stopped)                                   | I  |
| 10      | T4 (WDA)                 | Test VO (RDS clock output)                                                     | I  |
| 11      | T5 (RSPT)                | Test VO (RDS data output)                                                      | I  |
| 16      | T6 (ERROR/STK/TP/BE1)    | Test VO (error status, regenerated carrier, TP, error block count outputs)     | I  |
| 17      | T7 (CORRECTION/IDTA/BE0) | Test VO (error correction status, SK detection, TA, error block count outputs) | I  |
| 18      | SYNC                     | Block synchronization output                                                   | O  |
| 19      | RDS-ID                   | RDS detection                                                                  | O  |
| 20      | DO                       | Data output                                                                    | O  |
| 21      | CL                       | Clock input                                                                    | I  |
| 22      | DI                       | Data input                                                                     | I  |
| 23      | CE                       | Chip enable                                                                    | I  |
| 24      | SYR                      | Synchronization and RAM address reset (active high)                            | I  |
| 14      | V <sub>DD</sub>          | Digital power supply (+5V)                                                     | -  |
| 15      | V <sub>SS</sub>          | Digital ground                                                                 | -  |

\* Normally the output pin, used as an I/O pin in test mode, which is not available to user applications.

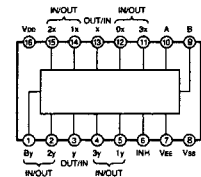
### IC412 KA7805R(Voltage Regulator)



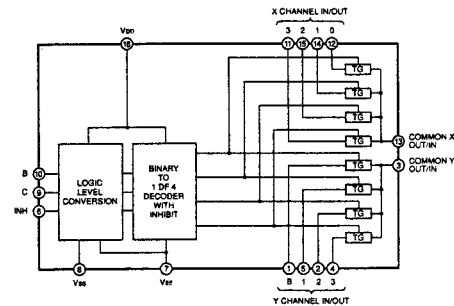
### IC410,411 PQ1CG21H2RZ(Chopper Regulator)



### IC450 CD4052BCM(Analog Multiplexer/)

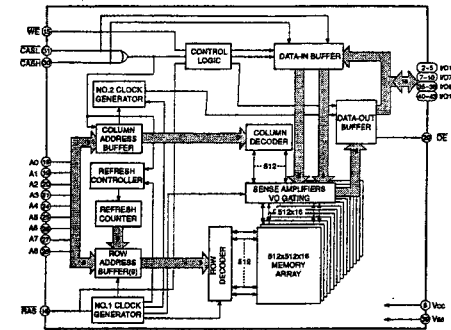


| INPUT STATES |   |   |   |   | *ON* CHANNELS |
|--------------|---|---|---|---|---------------|
| INHIBIT      | C | B | A |   | CD4052S       |
| 0            | 0 | 0 | 0 | 1 | 0X, 0Y        |
| 0            | 0 | 0 | 1 | 1 | 1X, 1Y        |
| 0            | 0 | 1 | 0 | 1 | 2X, 2Y        |
| 0            | 0 | 1 | 1 | 1 | 3X, 3Y        |
| 0            | 1 | 0 | 0 | 0 |               |
| 0            | 1 | 0 | 1 | 0 |               |
| 0            | 1 | 1 | 0 | 0 |               |
| 0            | 1 | 1 | 1 | 0 |               |
| 1            | - | - | - | - | NONE          |



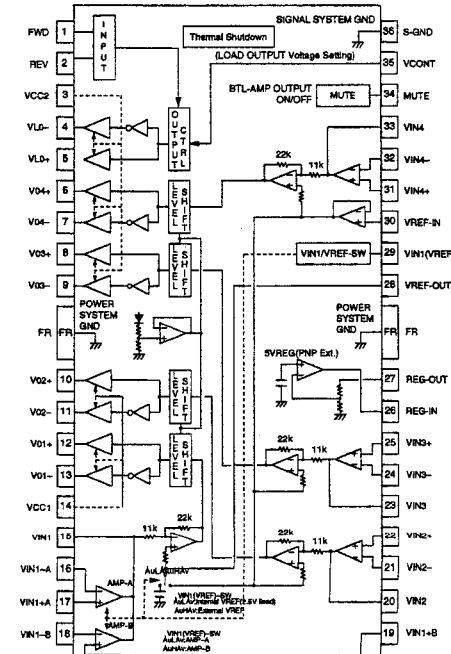
## IC BLOCK DIAGRAM & DESCRIPTION

### IC141 T224162B-35S(DRAM)

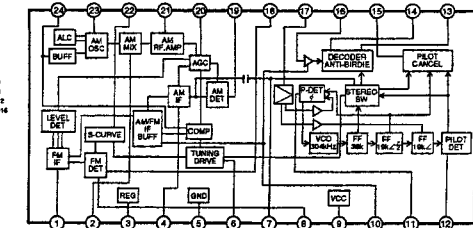


| Pin No.                                                                                                                                                                                                                                                                                                                                                                    | Symbol          | Type         | Description            |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------|--------------|------------------------|
| 14-18, 22-26                                                                                                                                                                                                                                                                                                                                                               | A0-A4           | Input        | Address Input          |
| 14                                                                                                                                                                                                                                                                                                                                                                         | RAS             | Input        | Row Address Strobe     |
| 26                                                                                                                                                                                                                                                                                                                                                                         | CAS             | Input        | Column Address Strobe  |
| 20                                                                                                                                                                                                                                                                                                                                                                         | CS              | Input        | Chip Select            |
| 13                                                                                                                                                                                                                                                                                                                                                                         | WE              | Input        | Write Enable           |
| 27                                                                                                                                                                                                                                                                                                                                                                         | OE              | Input        | Output Enable          |
| 24-26, 30-32, 34-36                                                                                                                                                                                                                                                                                                                                                        | D0-D15          | Input/Output | Data Input/Output      |
| 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 15, 16, 17, 18, 19, 20, 21, 23, 24, 25, 27, 28, 29, 31, 33, 35, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, 71, 72, 73, 74, 75, 76, 77, 78, 79, 80, 81, 82, 83, 84, 85, 86, 87, 88, 89, 90, 91, 92, 93, 94, 95, 96, 97, 98, 99, 100 | V <sub>DD</sub> | Supply       | Power, V <sub>DD</sub> |
| 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 15, 16, 17, 18, 19, 20, 21, 23, 24, 25, 27, 28, 29, 31, 33, 35, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, 71, 72, 73, 74, 75, 76, 77, 78, 79, 80, 81, 82, 83, 84, 85, 86, 87, 88, 89, 90, 91, 92, 93, 94, 95, 96, 97, 98, 99, 100 | V <sub>SS</sub> | Ground       | Ground                 |
| 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 15, 16, 17, 18, 19, 20, 21, 23, 24, 25, 27, 28, 29, 31, 33, 35, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, 71, 72, 73, 74, 75, 76, 77, 78, 79, 80, 81, 82, 83, 84, 85, 86, 87, 88, 89, 90, 91, 92, 93, 94, 95, 96, 97, 98, 99, 100 | NC              | No Connect   | No Connect             |

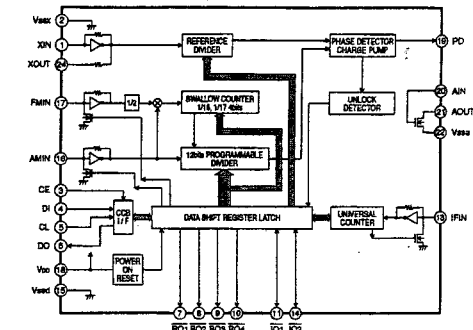
### IC160 LA6560(Motor Driver)



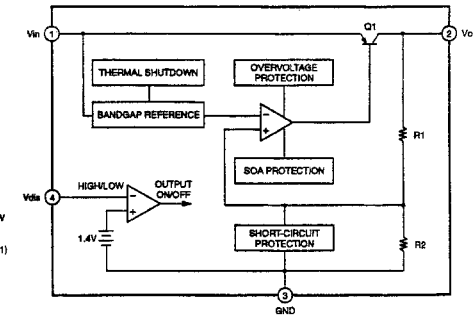
### IC231 LA1844ML(AM/FM-IF/MPX)



### IC241 LC72121M-D(PLL)



### IC402 KA78R12STU(Low Dropout Voltage Regulator)



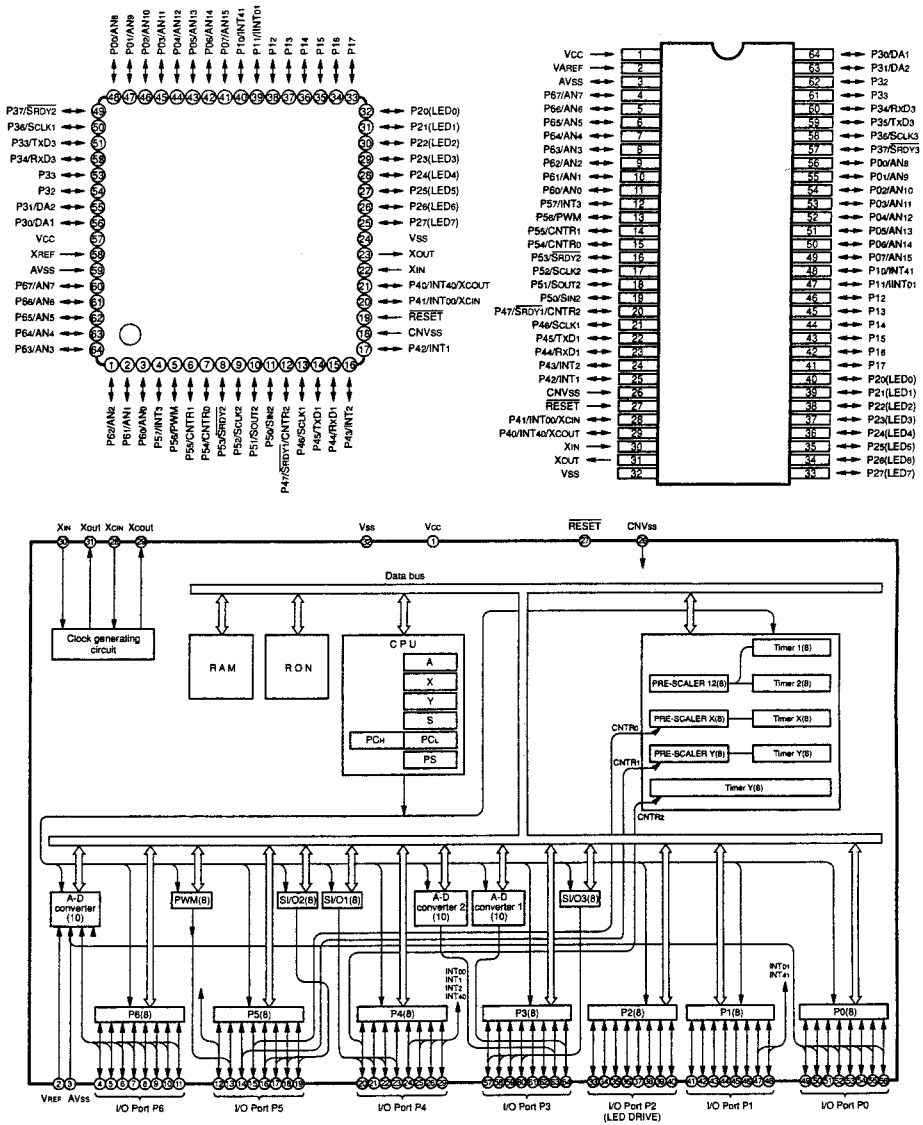
IC BLOCK DIAGRAM & DESCRIPTION

IC430 M38039MC-07FP(Single Chip 8-Bits Microcomputer)

| PIN NAME                                        | DESCRIPTION               | FANCTION                                                                                                                                                                                            | OTHER FUNCTION                                                                          |
|-------------------------------------------------|---------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------|
| VCC,VSS                                         | Power source input        | Impressed 2.7~5.5V to Vcc and 0V to Vss.                                                                                                                                                            |                                                                                         |
| CNVSS                                           | CNVSS                     | Controlled mode of operation. Connect to Vss.                                                                                                                                                       |                                                                                         |
| VREF                                            | Voltage reference input   | For A-D Converter and voltage reference.                                                                                                                                                            |                                                                                         |
| AVSS                                            | Analog power source input | For A-D converter and analog power source input. Connect to Vss.                                                                                                                                    |                                                                                         |
| RESET                                           | Reset input               | For active "L" reset.                                                                                                                                                                               |                                                                                         |
| XIN                                             | Clock input               | Clock generation I/O. Connect ceramic resonator or crystal oscillator between XIN and XOUT. Connect clock generator to XIN when outer clock used and XOUT is open. Feedback resistance is internal. |                                                                                         |
| XOUT                                            | Clock output              |                                                                                                                                                                                                     |                                                                                         |
| P00/AN6~<br>P07/AN15                            | I/O Port P0               | 8 bit I/O port. Possible appointment of I/O, bit unit.<br>Output formal is CMOS3 state.                                                                                                             | A-D Converter in                                                                        |
| P10/INT01<br>P11/INT41                          | I/O Port P1               | Possible pullup control, bit unit.<br>P20~P27 : Possible large current for LED drive.                                                                                                               | interruption in                                                                         |
| P12~P17                                         |                           |                                                                                                                                                                                                     |                                                                                         |
| P20~P27                                         | I/O Port P2               |                                                                                                                                                                                                     |                                                                                         |
| P30/DA1<br>P31/DA2                              | I/O Port P3               | 8 bit I/O port. Possible appointment of I/O, bit unit.<br>Input level is CMOS input level.                                                                                                          | D-A Converter out                                                                       |
| P32,P33                                         |                           | Output formal are CMOS3 state of P30,P31,P34~P37.                                                                                                                                                   |                                                                                         |
| P34/RxD3<br>P35/TxD3<br>P36/SCLK3<br>P37/SRDY3  |                           | Output formal are channel oper drain of P32,P33.<br>Other P32,P33 : Possible pullup control, bit unit.                                                                                              | Serial I/O3                                                                             |
| P40/INT40/XCOUT<br>P41/INT00/XCIN<br>P42/INT1   | I/O Port P4               | 8 bit I/O port. Possible appointment of I/O, bit unit.<br>CMOS input level : Output formal is CMOS3 state.<br>Possible pullup control, bit unit.                                                    | Interruption in<br>Sub-clock generation I/O<br>(Connected resonator)<br>Interruption in |
| P43/INT2<br>P44/RxD1<br>P45/TxD1<br>P46/SCLK1   |                           |                                                                                                                                                                                                     | Serial I/O1                                                                             |
| P47/SRDY1/CNTR2                                 |                           |                                                                                                                                                                                                     | Serial I/O1, timer Z                                                                    |
| P50/SIN2<br>P51/SOUT2<br>P52/SCLK2<br>P53/SRDY2 | I/O Port P5               | 8 bit I/O port. Possible appointment of I/O, bit unit.<br>CMOS input level : Output formal is CMOS3 state.<br>Possible pullup control, bit unit.                                                    | Serial I/O2                                                                             |
| P54/CNTR0<br>P55/CNTR1<br>P56/PWM<br>P57/INT3   |                           |                                                                                                                                                                                                     | Timer X<br>Timer Y<br>DWM out<br>Interruption in                                        |
| P60/AN0~<br>P67/AN7                             | I/O Port P6               |                                                                                                                                                                                                     | A-D Converter in                                                                        |

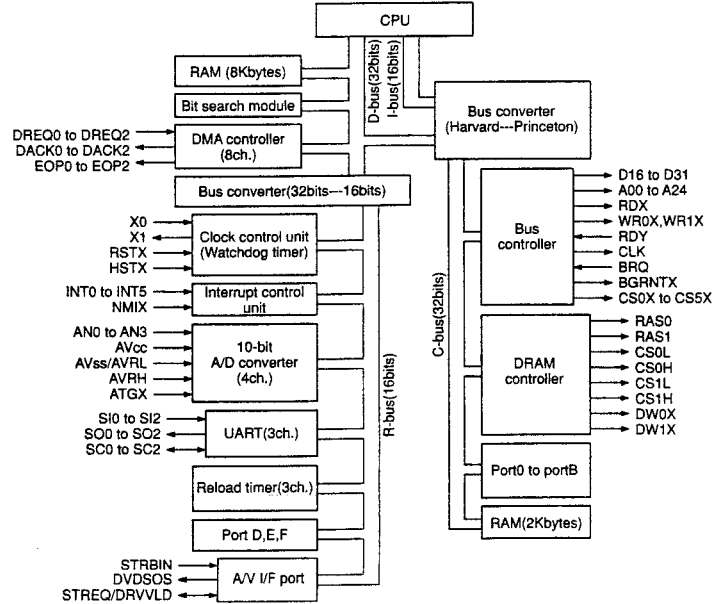
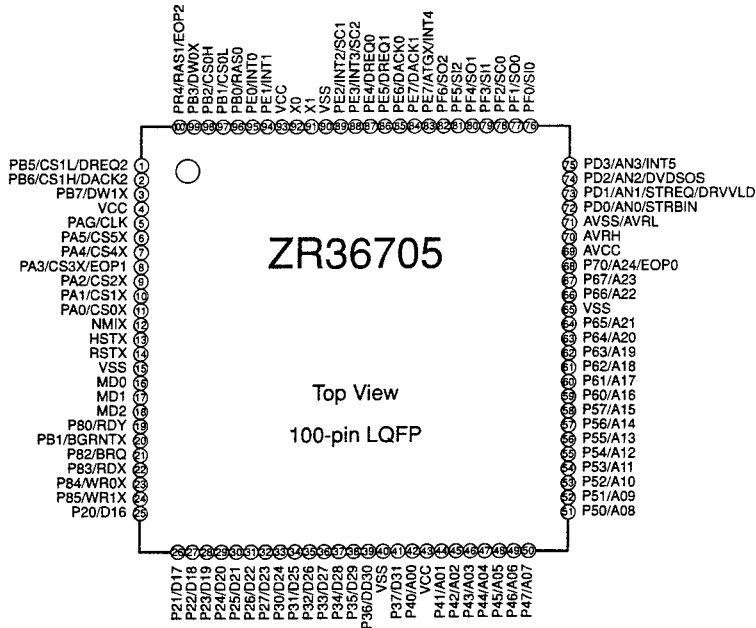
IC BLOCK DIAGRAM & DESCRIPTION

IC430 M38039MC-07FP(Single Chip 8-Bits Microcomputer)



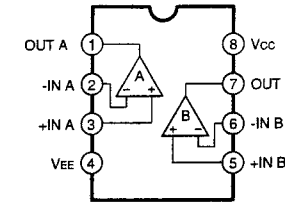
## IC BLOCK DIAGRAM & DESCRIPTION

### IC800 ZR36705TQC (Micro Controller)

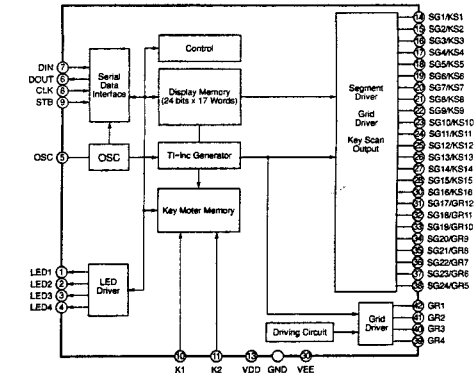


## IC BLOCK DIAGRAM & DESCRIPTION

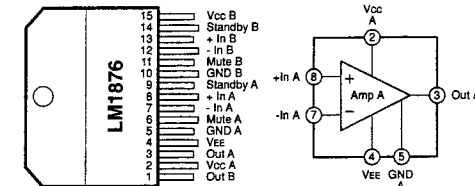
### IC460,461,470,471,480,481,490,495 KIA4558F, NJM4558M (Dual Low Noise Operational Amplifier)



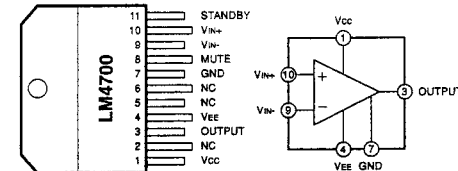
### IC601 PT6315 (VFD Driver/Controller)



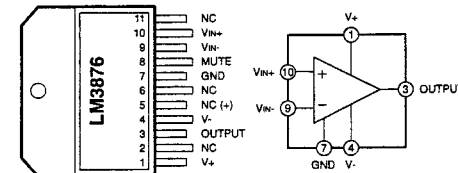
### IC462,472 LM1876 (Dual 20W audio Power Amplifier)



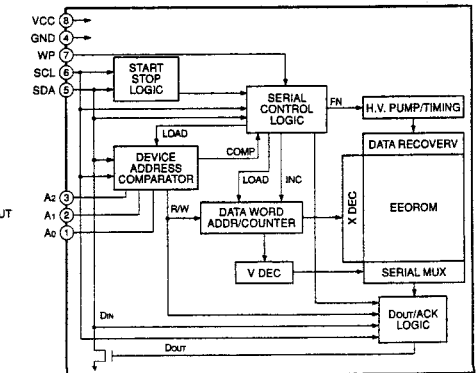
### IC482 LM4700TF (30w audio Power Amplifier)



### IC483 LM3876TF (56w audio Power Amplifier)



### IC801 AT24C02N-10SI-2.7 (EEPROM)





## IC BLOCK DIAGRAM & DESCRIPTION

### IC800 ZR36705TQC (Micro Controller)

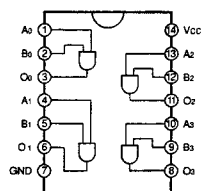
| Pin Number                                                                                   | Pin Name                                                                                                                                                                     | I/O Circuit Format | Function                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|----------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 25<br>26<br>27<br>28<br>29<br>30<br>31<br>32                                                 | D16/P20<br>D17/P21<br>D18/P22<br>D19/P23<br>D20/P24<br>D21/P25<br>D22/P26<br>D23/P27                                                                                         | E                  | Bits 16 to 23 of external data bus.<br>When the external bus width is set to 8 bits, these pins can be used as general-purpose I/O ports (P20 to P27).                                                                                                                                                                                                                                                                                      |
| 33<br>34<br>35<br>36<br>37<br>38<br>39<br>41                                                 | D24/P30<br>D25/P31<br>D26/P32<br>D27/P33<br>D28/P34<br>D29/P35<br>D30/P36<br>D31/P37                                                                                         | E                  | Bits 24 to 31 of external data bus.<br>When these pins are not used for the data bus, they can be used as general-purpose I/O ports (P30 to P37).                                                                                                                                                                                                                                                                                           |
| 42<br>44<br>45<br>46<br>47<br>48<br>49<br>50<br>51<br>52<br>53<br>54<br>55<br>56<br>57<br>58 | A00/P40<br>A01/P41<br>A02/P42<br>A03/P43<br>A04/P44<br>A05/P45<br>A06/P46<br>A07/P47<br>A08/P50<br>A09/P51<br>A10/P52<br>A11/P53<br>A12/P54<br>A13/P55<br>A14/P56<br>A15/P57 | F                  | Bits 00 to 15 of external address bus.<br>When these pins are not used for the address bus, they can be used as general-purpose I/O ports (P40 to P47 and P50 to P57).                                                                                                                                                                                                                                                                      |
| 59<br>60<br>61<br>62<br>63<br>64<br>65<br>66<br>67                                           | A16/P60<br>A17/P61<br>A18/P62<br>A19/P63<br>A20/P64<br>A21/P65<br>A22/P66<br>A23/P67                                                                                         | F                  | Bits 16 to 23 of external address bus.<br>When these pins are not used for the address bus, they can be used as general-purpose I/O ports (P60 to P67).                                                                                                                                                                                                                                                                                     |
| 68                                                                                           | A24/P70/EOP0                                                                                                                                                                 | F                  | Bits 24 of external address bus.<br>[EOP0] DMAC EOP output (ch 0). This function is valid when DMAC EOP output is enabled.<br>[P70] When this pin is not used as A24 and EOP0, the pin can be used as a general-purpose I/O port.                                                                                                                                                                                                           |
| 89                                                                                           | INT2/SC1/PE2                                                                                                                                                                 | F                  | [INT2] Input of external interrupt request. This input is used from time to time while the corresponding external interrupt is enabled. Therefore, it is needed to stop output by other functions except when such output is performed intentionally.<br>[SC1] UART1 clock I/O. Clock output can be used when UART1 clock output is enabled.<br>[PE2] General-purpose I/O port. This function is valid when UART1 clock output is disabled. |
| 88                                                                                           | INT3/SC2/PE3                                                                                                                                                                 | F                  | [INT3] Input of external interrupt request. This input is used from time to time while the corresponding external interrupt is enabled. Therefore, it is needed to stop output by other functions except when such output is performed intentionally.<br>[SC2] UART1 clock I/O. Clock output can be used when UART1 clock output is enabled.<br>[PE3] General-purpose I/O port. This function is valid when UART1 clock output is disabled. |
| 87<br>86                                                                                     | DREQ0/PE4<br>DREQ1/PE5                                                                                                                                                       | F                  | [DREQ0,1] Input of DMA external transfer request. This input is used from time to time when this pin is selected for the DMAC transfer cause. Therefore, it is needed to stop output by other functions except when such output is performed intentionally.<br>[PE4,5] General-purpose I/O ports.                                                                                                                                           |
| 85                                                                                           | DACK0/PE6                                                                                                                                                                    | F                  | [DACK0] Output of DMAC external transfer request acceptance (ch 0). This function is valid the output of DMAC transfer request acceptance is enabled.<br>[PE6] General-purpose I/O port. This function is valid when the output of DMAC transfer request acceptance or DACK0 output is disabled.                                                                                                                                            |
| 84                                                                                           | DACK1/PE7                                                                                                                                                                    | F                  | [DACK1] Output of DMAC external transfer request acceptance (ch 0). This function is valid when the output of DMAC transfer request acceptance is enabled.<br>[PE7] General-purpose I/O port. This function is valid when the output of DMAC transfer request acceptance or DACK0 output is disabled.                                                                                                                                       |
| 76                                                                                           | S10/PE0                                                                                                                                                                      | F                  | [S10] UART0 data input. This input is used from time to time while input operation is selected. Therefore, it is needed to stop output by other functions except when such output is performed intentionally.<br>[PF0] General-purpose I/O port.                                                                                                                                                                                            |
| 77                                                                                           | SO0/PF1                                                                                                                                                                      | F                  | [SO0] UART0 data output. This function is valid when UART0 data output is enabled.<br>[PF1] General-purpose I/O port. This function is valid when UART0 data output is disabled.                                                                                                                                                                                                                                                            |

## IC BLOCK DIAGRAM & DESCRIPTION

### IC800 ZR36705TQC (Micro Controller)

| Pin Number    | Pin Name                         | I/O Circuit Format | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|---------------|----------------------------------|--------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 19            | RDY/P80                          | E                  | External Ready input, 0 is input when the bus cycle being executed is not completed.<br>When the pin is not used for this purpose, it can be used as a general-purpose I/O port.                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 20            | BGRNTX/P81                       | F                  | Output of external bus release acceptance. L is output when the external bus has been released.<br>When the pin is not used for this purpose, it can be used as a general-purpose I/O port.                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 21            | BRQ/P82                          | E                  | Input of external bus release request. 1 is input to request that the external bus be released.<br>When the pin is not used for this purpose, it can be used as a general-purpose I/O port.                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 22            | RDX/P83                          | F                  | External bus read strobe.<br>When this pin is not used for this purpose, it can be used as general-purpose I/O port.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 23<br>24      | WR0X/P84<br>WR1X/P85             | F                  | External bus write strobes. Individual control signals and data bus byte positions have the following relationships.<br>For 16-bit bus width: WR0X strobes D15:D08<br>WR1X strobes D07:D00<br>For 8-bit bus width: WR0X strobes D15:D08<br>WR1 used as P85<br>Note: WR1X is Hi-Z while it is in reset state. When it is used as a 16-bit bus, attach a pull-up resistor to the outside.<br>[P84 or P85] When WR0X or WR1X is not used, the pin can be used as a general-purpose I/O port.                                                                                                                      |
| 11<br>10<br>9 | CS0X/PA0<br>CS1X/PA1<br>CS2X/PA2 | F                  | Chip Select 0 output (active-low)<br>Chip Select 1 output (active-low)<br>Chip Select 2 output (active-low)<br>[PA0,1 or 2] When the pin is not used for the above purpose, it can be used as a general-purpose I/O port.                                                                                                                                                                                                                                                                                                                                                                                      |
| 8             | CS3X/PA3/EOP1                    | F                  | Chip Select 3 output (active-low)<br>[EOP1] DMAC EOP1 output (ch 1). This function is valid when DMAC EOP output is enabled.<br>[PA3] When CS3X and EOP1 are not used, the pin can be used as a general-purpose I/O port.                                                                                                                                                                                                                                                                                                                                                                                      |
| 7<br>6        | CS4X/PA4<br>CS5X/PA5             | F                  | Chip Select 4 output (active-low)<br>Chip Select 5 output (active-low)<br>[PA4 or 5] When the pin is not used for the above purpose, it can be used as a general-purpose I/O port.                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 73            | AN1/STREQ /DRVV<br>LD/PD1        | G                  | [AN1] A/D converter analog input. This input is used from time to time while input operation is selected. Therefore, it is needed to stop output by other functions except when such output is performed intentionally.<br>[STREQ] STREQ output. This function is valid when STREQ output is enabled.<br>[PD1] General-purpose I/O port. This function is valid when STREQ output is disabled.<br>[DRVVLD] DRVVLD input. This input is used from time to time while input operation is selected. Therefore, it is needed to stop output by other functions except when such output is performed intentionally. |
| 74            | AN2/DVDSOS /PD2                  | G                  | [AN2] A/D converter analog input. This input is used from time to time while input operation is selected. Therefore, it is needed to stop output by other functions except when such output is performed intentionally.<br>[DVDSOS] DVDSOS output. This function is valid when DVDSOS output is enabled.<br>[PD2] General-purpose I/O port. This function is valid when DVDSOS output is disabled.                                                                                                                                                                                                             |
| 75            | AN3/INT5/PD3                     | G                  | [AN3] A/D converter analog input. This input is used from time to time while input operation is selected. Therefore, it is needed to stop output by other functions except when such output is performed intentionally.<br>[INT5] Input of external interrupt request. This input is used from time to time while the corresponding external interrupt is enabled. Therefore, it is needed to stop output by other functions except when such output is performed intentionally.<br>[PD3] General-purpose I/O port.                                                                                            |
| 69            | AVCC                             | -                  | VCC power supply for A/D converter.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 70            | AVRH                             | -                  | Reference voltage of A/D converter (high potential side).<br>Always turn the pin on or off while the voltage equal to AVCC or higher is applied to VCC.                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 71            | AVSS/AVRL                        | -                  | A/D converter VSS power supply and reference voltage (low potential side).                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 4,43,93       | VCC                              | -                  | Digital circuit power supply. Be sure to connect the power supply to every VCC pin.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 15,40,65,90   | VSS                              | -                  | Digital circuit ground level.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 78            | SC0/PF2                          | F                  | [SC0] UART0 clock I/O. Clock output can be used when UART0 clock output is enabled.<br>[PF2] General-purpose I/O port. This function is valid when UART0 clock output is disabled.                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 79            | SI1/PF3                          | F                  | [SI1] UART1 data input. This input is used from time to time while input operation is selected. Therefore, it is needed to stop output by other functions except when such output is performed intentionally.<br>[PF3] General-purpose I/O port.                                                                                                                                                                                                                                                                                                                                                               |
| 80            | SO1/PF4                          | F                  | [SO1] UART1 data output. This function is valid when UART1 data output is enabled.<br>[PF4] General-purpose I/O port. This function is valid when UART1 data output is disabled.                                                                                                                                                                                                                                                                                                                                                                                                                               |

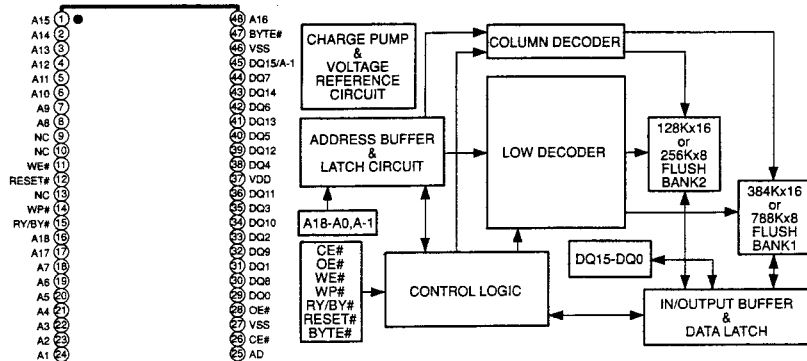
**IC806 74VHCT08A (Quad 2-Input AND Gate)**



| A | B | O |
|---|---|---|
| L | L | L |
| L | H | L |
| H | L | L |
| H | H | H |

| Pin Names                     | Description |
|-------------------------------|-------------|
| A <sub>1</sub> B <sub>1</sub> | Inputs      |
| O <sub>1</sub>                | Outputs     |

A15 ① ●



| Symbols    | Pin Name                  | Functions                                                                                                                                                                       |
|------------|---------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| A18,A17    | Bank Selective Address    | Selects bank 1 when "L" and bank 2.                                                                                                                                             |
| A16-A0,A-1 | Flush Bank Address        | Supply address for flush bank.                                                                                                                                                  |
| A18-A15    | Flush Bank Block Address  | Select flush bank for erase.                                                                                                                                                    |
| A18-A10    | Flush Bank Sector Address | Select flush bank sector for erase.                                                                                                                                             |
| DO15-DO0   | Data input/Output         | To output data during read cycle and receive input data during write cycles. Data is internally latched during a writecycle. The output are high impedance when OE#,CE# is "H". |
| CE#        | Chip Enable               | To activate the flush bank when CE# is "L".                                                                                                                                     |
| OE#        | Output Enable             | To activate the data output buffer .                                                                                                                                            |
| WE#        | Write Enable              | To control the write, erase and program.                                                                                                                                        |
| BYTE#      | Bait Pin                  | Bait mode when "L" and word mode when "H".                                                                                                                                      |
| RY/BY#     | Ladey/Beje Output         | Output "L" when write and except "H".                                                                                                                                           |
| WP#        | Write Protect             | To activate hardware write protect when "L".                                                                                                                                    |
| RESET#     | Reset                     | To activate hardware reset when "L".                                                                                                                                            |
| VDD        | Power Supply              | 2.7V~3.6V supply.                                                                                                                                                               |
| VSS        | Ground                    |                                                                                                                                                                                 |

**IC800 ZR36705TQC (Micro Controller)**

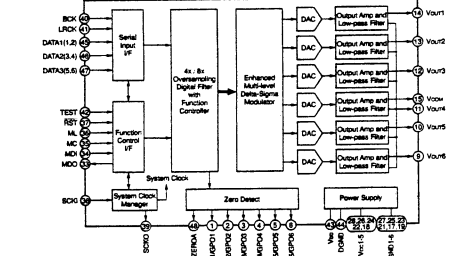
| Pin Number                  | Pin Name                                                      | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|-----------------------------|---------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 81                          | SI2/PF5                                                       | [SI2] UART2 data input. This input is used from time to time while input operation is selected. Therefore, it is needed to stop output by other functions except when such output is performed intentionally.<br>[PF5] General-purpose I/O port.                                                                                                                                                                                                                                                                                                   |
| 82                          | SO2/PF6                                                       | [SO2] UART2 data output. This function is valid when UART2 data output is enabled.<br>[PF6] General-purpose I/O port. This function is valid when UART2 data output is disabled.                                                                                                                                                                                                                                                                                                                                                                   |
| 83                          | PF7/INT4/ATGX                                                 | [INT4] Input of external interrupt request. This input is used from time to time while the corresponding external interrupt is enabled. Therefore, it is needed to stop output by other functions except when such output is performed intentionally.<br>[ATGX] External trigger input for A/D converter. This input is used from time to time when this pin is selected for the A/D start cause. Therefore, it is needed to stop output by other functions except when such output is performed intentionally.<br>[PF7] General-purpose I/O port. |
| 72                          | AN0/STRBIN /PD0                                               | [AN0] A/D converter analog input. This input is used from time to time while input operation is selected. Therefore, it is needed to stop output by other functions except when such output is performed intentionally.<br>[STRBIN] The clocksource input for DVDSOS logic. This input is used from time to time while input operation is selected. Therefore, it is needed to stop output by other functions except when such output is performed intentionally.<br>[PD0] General-purpose I/O port.                                               |
| 5                           | CLK/PA6                                                       | System clock output. The pin outputs the same clock frequency as the external bus operating frequency.<br>[PA6] When the pin is not used for this purpose, it can be used as a general-purpose I/O port.                                                                                                                                                                                                                                                                                                                                           |
| 96<br>97<br>98<br>99<br>100 | RAS0/PB0<br>CS0H/PB1<br>CS0H/PB2<br>DW0X/PB3<br>RAS1/PB4/EOP2 | RAS output of DRAM bank 0<br>CASL output of DRAM bank 0<br>CASH output of DRAM bank 0<br>WE output of DRAM bank 0<br>RAS output of DRAM bank 1<br>CASL output of DRAM bank 1<br>CASH output of DRAM bank 1<br>WE output of DRAM bank 1                                                                                                                                                                                                                                                                                                             |
| 1                           | CS1H/PB5 /DREQ2                                               | See the description of the DRAM interface for more information.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 2                           | CS1H/PB6 /DACK2                                               | [EOP2] DMAC EOP output (ch 2). This function is valid when DMAC EOP output is enabled.                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 3                           | DW1X/PB7                                                      | [DREQ2] Input of DMA external transfer request. This input is used from time to time when this pin is selected for the DMAC transfer cause. Therefore, it is needed to stop output by other functions except when such output is performed intentionally.<br>[DACK2] Output of DMAC external transfer request acceptance (ch 2). This function is valid when the output of DMAC transfer request acceptance is enabled.<br>[PB0-7] When each pin is not used for the corresponding purpose, the pin can be used as a general-purpose I/O port.     |
| 16<br>17<br>18              | MD0<br>MD1<br>MD2                                             | Mode pins 0 to 2. Use these pins to setting the basic MCU operation Mode.<br>Connect these pins directly to Vcc or Vss.                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 92<br>91                    | X0<br>X1                                                      | Clock (Oscillator) input<br>Clock (Oscillator) output                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 14                          | RSTX                                                          | External reset input.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 13                          | HSTX                                                          | Hardware Standby input.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 12                          | NMIX                                                          | Non-maskable interrupt (NMI) input (active-low).                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 95<br>94                    | INT0/PE0<br>INT1/PE1                                          | [INT0,1] Input of external interrupt request. This input is used from time to time while the corresponding external interrupt is enabled. Therefore, it is needed to stop output by other functions except when such output is performed intentionally.<br>[PE0,1] General-purpose I/O ports.                                                                                                                                                                                                                                                      |

# IC BLOCK DIAGRAM & DESCRIPTION

## IC820 ZR36732 (MPEG)

| Pin                                                      | Name       | Type | Direction | Status After RESET/<br>During STANDBY      |
|----------------------------------------------------------|------------|------|-----------|--------------------------------------------|
| SDRAM interface (35 pins)                                |            |      |           |                                            |
| 90                                                       | RAMDAT[15] | 3-S  | IO (I)    | Reset: input (p.d.)<br>Standby: 3-S (p.d.) |
| 91                                                       | RAMDAT[14] |      |           |                                            |
| 92                                                       | RAMDAT[13] |      |           |                                            |
| 93                                                       | RAMDAT[12] |      |           |                                            |
| 94                                                       | RAMDAT[11] |      |           |                                            |
| 95                                                       | RAMDAT[10] |      |           |                                            |
| 96                                                       | RAMDAT[9]  |      |           |                                            |
| 97                                                       | RAMDAT[8]  |      |           |                                            |
| 98                                                       | RAMDAT[7]  |      |           |                                            |
| 99                                                       | RAMDAT[6]  |      |           |                                            |
| 100                                                      | RAMDAT[5]  |      |           |                                            |
| 101                                                      | RAMDAT[4]  |      |           |                                            |
| 102                                                      | RAMDAT[3]  |      |           |                                            |
| 103                                                      | RAMDAT[2]  |      |           |                                            |
| 104                                                      | RAMDAT[1]  |      |           |                                            |
| 105                                                      | RAMDAT[0]  |      |           |                                            |
| SDRAM bidirectional data bus                             |            |      |           |                                            |
| 55                                                       | RAMAD[15]  | O    | O (p.d.)  | Reset: output<br>Standby: 3-S              |
| 56                                                       | RAMAD[14]  |      |           |                                            |
| 57                                                       | RAMAD[13]  |      |           |                                            |
| 58                                                       | RAMAD[12]  |      |           |                                            |
| 59                                                       | RAMAD[11]  |      |           |                                            |
| 60                                                       | RAMAD[10]  |      |           |                                            |
| 61                                                       | RAMAD[9]   |      |           |                                            |
| 62                                                       | RAMAD[8]   |      |           |                                            |
| 63                                                       | RAMAD[7]   |      |           |                                            |
| 64                                                       | RAMAD[6]   |      |           |                                            |
| 65                                                       | RAMAD[5]   |      |           |                                            |
| 66                                                       | RAMAD[4]   |      |           |                                            |
| 67                                                       | RAMAD[3]   |      |           |                                            |
| 68                                                       | RAMAD[2]   |      |           |                                            |
| 69                                                       | RAMAD[1]   |      |           |                                            |
| 70                                                       | RAMAD[0]   |      |           |                                            |
| SDRAM clock output (Same as internal processing clock)   |            |      |           |                                            |
| 81                                                       | RAMCLK     | O    | O (p.d.)  | Reset: output<br>Standby: 3-S (p.d.)       |
| SDRAM row select output                                  |            |      |           |                                            |
| 82                                                       | RAS        | O    | O (p.d.)  | Reset: output<br>Standby: 3-S (p.d.)       |
| SDRAM column select output                               |            |      |           |                                            |
| 83                                                       | CS         | O    | O (p.d.)  | Reset: output<br>Standby: 3-S (p.d.)       |
| SDRAM data strobe output                                 |            |      |           |                                            |
| 84                                                       | WE         | O    | O (p.d.)  | Reset: output<br>Standby: 3-S (p.d.)       |
| SDRAM data masking output                                |            |      |           |                                            |
| 85                                                       | DM         | O    | O (p.d.)  | Reset: output<br>Standby: 3-S (p.d.)       |
| SDRAM chip select output for the lower 2MB device (16MB) |            |      |           |                                            |
| 86                                                       | RAS        | O    | O (p.d.)  | Reset: output<br>Standby: 3-S (p.d.)       |
| SDRAM chip select output for the upper 2MB device (16MB) |            |      |           |                                            |
| 87                                                       | RAS        | O    | O (p.d.)  | Reset: output<br>Standby: 3-S (p.d.)       |
| SDRAM write enable output                                |            |      |           |                                            |
| 88                                                       | WE         | O    | O (p.d.)  | Reset: output<br>Standby: 3-S (p.d.)       |

## IC870 PCM1602Y (Digital to Analog Controller)



| Pin             | Name  | Type | Direction | Status After RESET/<br>During STANDBY |
|-----------------|-------|------|-----------|---------------------------------------|
| PIN ASSIGNMENTS |       |      |           |                                       |
| 1               | TEST  | I    |           |                                       |
| 2               | RESET | I    |           |                                       |
| 3               | MODE  | I    |           |                                       |
| 4               | MODE  | I    |           |                                       |
| 5               | MODE  | I    |           |                                       |
| 6               | MODE  | I    |           |                                       |
| 7               | MODE  | I    |           |                                       |
| 8               | MODE  | I    |           |                                       |
| 9               | MODE  | I    |           |                                       |
| 10              | MODE  | I    |           |                                       |
| 11              | MODE  | I    |           |                                       |
| 12              | MODE  | I    |           |                                       |
| 13              | MODE  | I    |           |                                       |
| 14              | MODE  | I    |           |                                       |
| 15              | MODE  | I    |           |                                       |
| 16              | MODE  | I    |           |                                       |
| 17              | MODE  | I    |           |                                       |
| 18              | MODE  | I    |           |                                       |
| 19              | MODE  | I    |           |                                       |
| 20              | MODE  | I    |           |                                       |
| 21              | MODE  | I    |           |                                       |
| 22              | MODE  | I    |           |                                       |
| 23              | MODE  | I    |           |                                       |
| 24              | MODE  | I    |           |                                       |
| 25              | MODE  | I    |           |                                       |
| 26              | MODE  | I    |           |                                       |
| 27              | MODE  | I    |           |                                       |
| 28              | MODE  | I    |           |                                       |
| 29              | MODE  | I    |           |                                       |
| 30              | MODE  | I    |           |                                       |
| 31              | MODE  | I    |           |                                       |
| 32              | MODE  | I    |           |                                       |
| 33              | MODE  | I    |           |                                       |
| 34              | MODE  | I    |           |                                       |
| 35              | MODE  | I    |           |                                       |
| 36              | MODE  | I    |           |                                       |
| 37              | MODE  | I    |           |                                       |
| 38              | MODE  | I    |           |                                       |
| 39              | MODE  | I    |           |                                       |
| 40              | MODE  | I    |           |                                       |
| 41              | MODE  | I    |           |                                       |
| 42              | MODE  | I    |           |                                       |
| 43              | MODE  | I    |           |                                       |
| 44              | MODE  | I    |           |                                       |
| 45              | MODE  | I    |           |                                       |
| 46              | MODE  | I    |           |                                       |
| 47              | MODE  | I    |           |                                       |
| 48              | MODE  | I    |           |                                       |
| 49              | MODE  | I    |           |                                       |
| 50              | MODE  | I    |           |                                       |
| 51              | MODE  | I    |           |                                       |
| 52              | MODE  | I    |           |                                       |
| 53              | MODE  | I    |           |                                       |
| 54              | MODE  | I    |           |                                       |
| 55              | MODE  | I    |           |                                       |
| 56              | MODE  | I    |           |                                       |
| 57              | MODE  | I    |           |                                       |
| 58              | MODE  | I    |           |                                       |
| 59              | MODE  | I    |           |                                       |
| 60              | MODE  | I    |           |                                       |
| 61              | MODE  | I    |           |                                       |
| 62              | MODE  | I    |           |                                       |
| 63              | MODE  | I    |           |                                       |
| 64              | MODE  | I    |           |                                       |
| 65              | MODE  | I    |           |                                       |
| 66              | MODE  | I    |           |                                       |
| 67              | MODE  | I    |           |                                       |
| 68              | MODE  | I    |           |                                       |
| 69              | MODE  | I    |           |                                       |
| 70              | MODE  | I    |           |                                       |
| 71              | MODE  | I    |           |                                       |
| 72              | MODE  | I    |           |                                       |
| 73              | MODE  | I    |           |                                       |
| 74              | MODE  | I    |           |                                       |
| 75              | MODE  | I    |           |                                       |
| 76              | MODE  | I    |           |                                       |
| 77              | MODE  | I    |           |                                       |
| 78              | MODE  | I    |           |                                       |
| 79              | MODE  | I    |           |                                       |
| 80              | MODE  | I    |           |                                       |
| 81              | MODE  | I    |           |                                       |
| 82              | MODE  | I    |           |                                       |
| 83              | MODE  | I    |           |                                       |
| 84              | MODE  | I    |           |                                       |
| 85              | MODE  | I    |           |                                       |
| 86              | MODE  | I    |           |                                       |
| 87              | MODE  | I    |           |                                       |
| 88              | MODE  | I    |           |                                       |
| 89              | MODE  | I    |           |                                       |
| 90              | MODE  | I    |           |                                       |
| 91              | MODE  | I    |           |                                       |
| 92              | MODE  | I    |           |                                       |
| 93              | MODE  | I    |           |                                       |
| 94              | MODE  | I    |           |                                       |
| 95              | MODE  | I    |           |                                       |
| 96              | MODE  | I    |           |                                       |
| 97              | MODE  | I    |           |                                       |
| 98              | MODE  | I    |           |                                       |
| 99              | MODE  | I    |           |                                       |
| 100             | MODE  | I    |           |                                       |
| 101             | MODE  | I    |           |                                       |
| 102             | MODE  | I    |           |                                       |
| 103             | MODE  | I    |           |                                       |
| 104             | MODE  | I    |           |                                       |
| 105             | MODE  | I    |           |                                       |
| 106             | MODE  | I    |           |                                       |
| 107             | MODE  | I    |           |                                       |
| 108             | MODE  | I    |           |                                       |
| 109             | MODE  | I    |           |                                       |
| 110             | MODE  | I    |           |                                       |
| 111             | MODE  | I    |           |                                       |
| 112             | MODE  | I    |           |                                       |
| 113             | MODE  | I    |           |                                       |
| 114             | MODE  | I    |           |                                       |
| 115             | MODE  | I    |           |                                       |
| 116             | MODE  | I    |           |                                       |
| 117             | MODE  | I    |           |                                       |
| 118             | MODE  | I    |           |                                       |
| 119             | MODE  | I    |           |                                       |
| 120             | MODE  | I    |           |                                       |
| 121             | MODE  | I    |           |                                       |
| 122             | MODE  | I    |           |                                       |
| 123             | MODE  | I    |           |                                       |
| 124             | MODE  | I    |           |                                       |
| 125             | MODE  | I    |           |                                       |
| 126             | MODE  | I    |           |                                       |
| 127             | MODE  | I    |           |                                       |
| 128             | MODE  | I    |           |                                       |
| 129             | MODE  | I    |           |                                       |
| 130             | MODE  | I    |           |                                       |
| 131             | MODE  | I    |           |                                       |
| 132             | MODE  | I    |           |                                       |
| 133             | MODE  | I    |           |                                       |
| 134             | MODE  | I    |           |                                       |
| 135             | MODE  | I    |           |                                       |
| 136             | MODE  | I    |           |                                       |
| 137             | MODE  | I    |           |                                       |
| 138             | MODE  | I    |           |                                       |
| 139             | MODE  | I    |           |                                       |
| 140             | MODE  | I    |           |                                       |
| 141             | MODE  | I    |           |                                       |
| 142             | MODE  | I    |           |                                       |
| 143             | MODE  | I    |           |                                       |
| 144             | MODE  | I    |           |                                       |
| 145             | MODE  | I    |           |                                       |
| 146             | MODE  | I    |           |                                       |
| 147             | MODE  | I    |           |                                       |
| 148             | MODE  | I    |           |                                       |
| 149             | MODE  | I    |           |                                       |
| 150             | MODE  | I    |           |                                       |
| 151             | MODE  | I    |           |                                       |
| 152             | MODE  | I    |           |                                       |
| 153             | MODE  | I    |           |                                       |
| 154             | MODE  | I    |           |                                       |
| 155             | MODE  | I    |           |                                       |
| 156             | MODE  | I    |           |                                       |
| 157             | MODE  | I    |           |                                       |
| 158             | MODE  | I    |           |                                       |
| 159             | MODE  | I    |           |                                       |
| 160             | MODE  | I    |           |                                       |
| 161             | MODE  | I    |           |                                       |
| 162             | MODE  | I    |           |                                       |
| 163             | MODE  | I    |           |                                       |
| 164             | MODE  | I    |           |                                       |
| 165             | MODE  | I    |           |                                       |
| 166             | MODE  | I    |           |                                       |
| 167             | MODE  | I    |           |                                       |
| 168             | MODE  | I    |           |                                       |
| 169             | MODE  | I    |           |                                       |
| 170             | MODE  | I    |           |                                       |
| 171             | MODE  | I    |           |                                       |
| 172             | MODE  | I    |           |                                       |
| 173             | MODE  | I    |           |                                       |
| 174             | MODE  | I    |           |                                       |
| 175             | MODE  | I    |           |                                       |
| 176             | MODE  | I    |           |                                       |
| 177             | MODE  | I    |           |                                       |
| 178             | MODE  | I    |           |                                       |
| 179             | MODE  | I    |           |                                       |
| 180             | MODE  | I    |           |                                       |
| 181             | MODE  | I    |           |                                       |
| 182             | MODE  | I    |           |                                       |
| 183             | MODE  | I    |           |                                       |
| 184             | MODE  | I    |           |                                       |
| 185             | MODE  | I    |           |                                       |
| 186             | MODE  | I    |           |                                       |
| 187             | MODE  | I    |           |                                       |
| 188             | MODE  | I    |           |                                       |
| 189             | MODE  | I    |           |                                       |
| 190             | MODE  | I    |           |                                       |
| 191             | MODE  | I    |           |                                       |
| 192             | MODE  | I    |           |                                       |
| 193             | MODE  | I    |           |                                       |
| 194             | MODE  | I    |           |                                       |
| 195             | MODE  | I    |           |                                       |
| 196             | MODE  | I    |           |                                       |
| 197             | MODE  | I    |           |                                       |
| 198             | MODE  | I    |           |                                       |
| 199             | MODE  | I    |           |                                       |
| 200             | MODE  | I    |           |                                       |

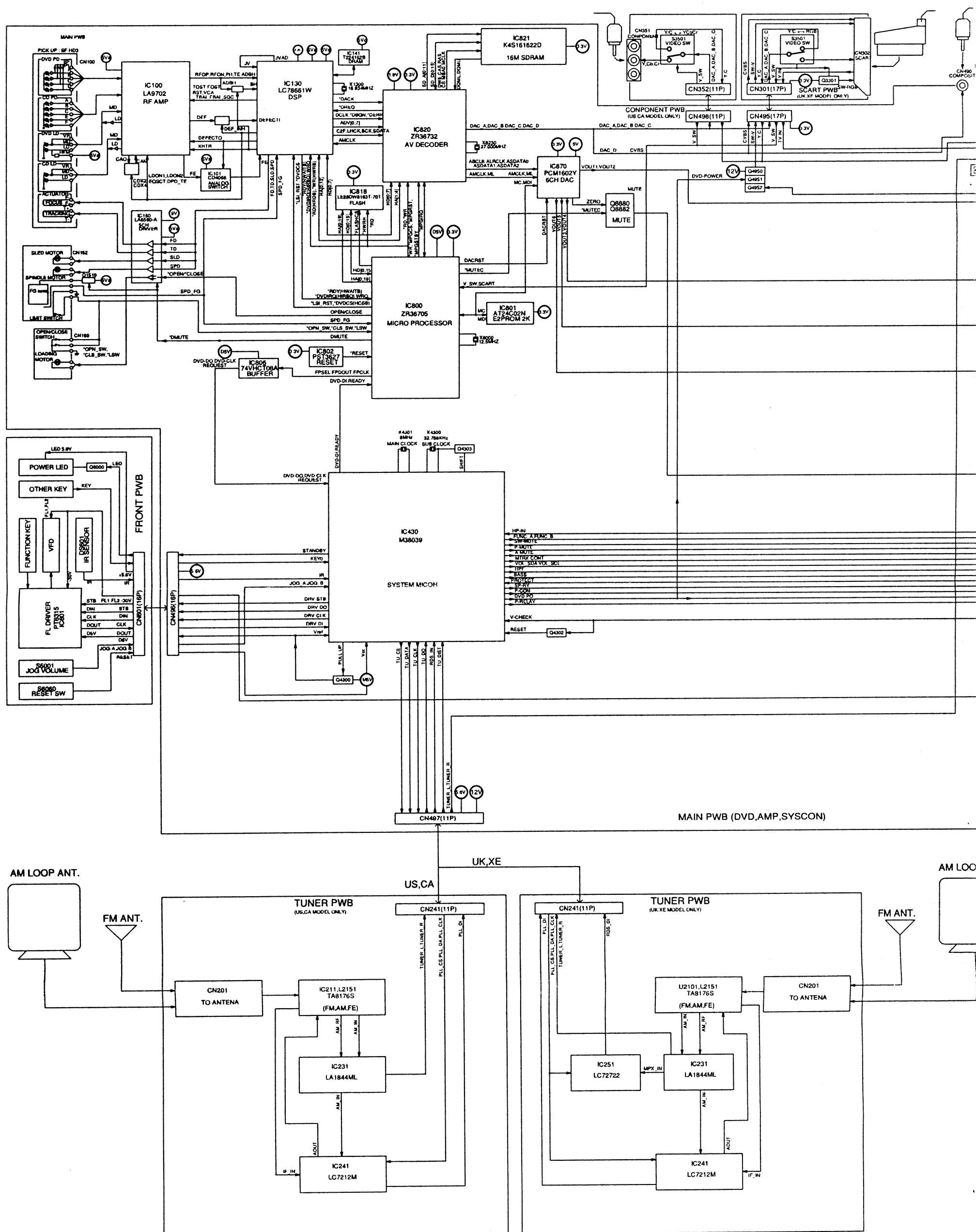
NOTES: (1) Schmitt-Trigger input with internal pull-down. (2) Schmitt-Trigger input. (3) Schmitt-Trigger output. (4) Tri-state output.

# IC BLOCK DIAGRAM & DESCRIPTION

## IC820 ZR36732 (MPEG)

| Pin                                                                                                                                                                                                                                                                                                                                                                                                                             | Name    | Type | Direction | Status After RESET/<br>During STANDBY       |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|------|-----------|---------------------------------------------|
| Test Signal Interface (3 pins)                                                                                                                                                                                                                                                                                                                                                                                                  |         |      |           |                                             |
| 17                                                                                                                                                                                                                                                                                                                                                                                                                              | HDP1    | 3-S  | IO (I)    | Reset: input (p.d.)                         |
| 18                                                                                                                                                                                                                                                                                                                                                                                                                              | HDP2    | 3-S  | IO (I)    | Standby: 3-S (p.d.)                         |
| 20                                                                                                                                                                                                                                                                                                                                                                                                                              | HDP3    | 3-S  | IO (I)    | Reset: input (p.d.)                         |
| 21                                                                                                                                                                                                                                                                                                                                                                                                                              | HDP4    | 3-S  | IO (I)    | Standby: 3-S (p.d.)                         |
| 22                                                                                                                                                                                                                                                                                                                                                                                                                              | HDP5    | 3-S  | IO (p.d.) | Reset: input (p.d.)                         |
| 23                                                                                                                                                                                                                                                                                                                                                                                                                              | HDP6    | 3-S  | IO (p.d.) | Standby: 3-S (p.d.)                         |
| 24                                                                                                                                                                                                                                                                                                                                                                                                                              | HDP7    | 3-S  | IO (I)    | Reset: input (p.d.)                         |
| 25                                                                                                                                                                                                                                                                                                                                                                                                                              | HDP8    | 3-S  | IO (I)    | Standby: 3-S (p.d.)                         |
| For 1-bit mode, the 8 I/O data lines of host data bus. For 1-bit mode, only these signals are defined as host data signals.                                                                                                                                                                                                                                                                                                     |         |      |           |                                             |
| 9                                                                                                                                                                                                                                                                                                                                                                                                                               | HDP11   | 3-S  | IO (p.d.) | Reset: input (low)                          |
| 11                                                                                                                                                                                                                                                                                                                                                                                                                              | HDP10   | 3-S  | IO (I)    | Standby: 3-S (p.d.)                         |
| 12                                                                                                                                                                                                                                                                                                                                                                                                                              | HDP9    | 3-S  | IO (I)    | Reset: input (low)                          |
| 13                                                                                                                                                                                                                                                                                                                                                                                                                              | HDP8    | 3-S  | IO (I)    | Standby: 3-S (p.d.)                         |
| When HDP10 is connected to VDDP, these data lines 1-8 are used for 1-bit host data bus. When HDP9 is connected to VDDP, these are the CD-RSP PS port outputs as explained in the CD-RSP pin description.                                                                                                                                                                                                                        |         |      |           |                                             |
| 6                                                                                                                                                                                                                                                                                                                                                                                                                               | HDP15   | 3-S  | IO (I)    | Reset: input (p.d.)                         |
| 7                                                                                                                                                                                                                                                                                                                                                                                                                               | HDP14   | 3-S  | IO (I)    | Standby: 3-S (p.d.)                         |
| 8                                                                                                                                                                                                                                                                                                                                                                                                                               | HDP13   | 3-S  | IO (I)    | Reset: input (p.d.)                         |
| 9                                                                                                                                                                                                                                                                                                                                                                                                                               | HDP12   | 3-S  | IO (I)    | Standby: 3-S (p.d.)                         |
| Host address inputs. These pins are used to indicate the register address in every cycle on the host interface.                                                                                                                                                                                                                                                                                                                 |         |      |           |                                             |
| 31                                                                                                                                                                                                                                                                                                                                                                                                                              | HDP30   | I    | Input     |                                             |
| 32                                                                                                                                                                                                                                                                                                                                                                                                                              | HDP29   | I    | Input     |                                             |
| 33                                                                                                                                                                                                                                                                                                                                                                                                                              | HDP28   | I    | Input     |                                             |
| In host protocol Type A (HDP15 ~ HDP27): HDP27 This input determines the direction of the host address.                                                                                                                                                                                                                                                                                                                         |         |      |           |                                             |
| 27                                                                                                                                                                                                                                                                                                                                                                                                                              | HDP27   | I    | Input     |                                             |
| 28                                                                                                                                                                                                                                                                                                                                                                                                                              | HDP26   | I    | Input     |                                             |
| 29                                                                                                                                                                                                                                                                                                                                                                                                                              | HDP25   | I    | Input     |                                             |
| 30                                                                                                                                                                                                                                                                                                                                                                                                                              | HDP24   | I    | Input     |                                             |
| In host protocol Type A (HDP15 ~ HDP27): HDP24 Data strobe input (active low).                                                                                                                                                                                                                                                                                                                                                  |         |      |           |                                             |
| 31                                                                                                                                                                                                                                                                                                                                                                                                                              | HDP23   | I    | Input     |                                             |
| In host protocol Type B (HDP15 ~ HDP27): HDP23 Data strobe input (active low).                                                                                                                                                                                                                                                                                                                                                  |         |      |           |                                             |
| 36                                                                                                                                                                                                                                                                                                                                                                                                                              | HDP17   | 3-S  | IO (p.d.) | Reset: output (low)<br>Standby: 3-S         |
| Host ready output. When this signal is set (p.d.), it requires a clock-up resistor, so to forcing. Confirmed as tri-state output can be written to the Decoder will be used to put in condition in standby. When HDP17 is low during a host access, the Decoder may be used to put in condition in standby. When HDP17 is high during a host access, the Decoder may be used to put in condition in standby.                    |         |      |           |                                             |
| 37                                                                                                                                                                                                                                                                                                                                                                                                                              | HDP16   | 3-S  | IO (p.d.) | Reset: output (high)<br>Standby: 3-S        |
| Interrupt request. This output signal requests an interrupt from the host controller. One of the events associated to interrupt occurs, and it is not masked. It is used to indicate the host request in the interrupt by sending the interrupt status register of the host decoder the interrupt, or after RESET.                                                                                                              |         |      |           |                                             |
| 39                                                                                                                                                                                                                                                                                                                                                                                                                              | HDP30   | 3-S  | IO (p.d.) | Reset: output (high)<br>Standby: 3-S        |
| Decoder of the HDP30 output from the host controller and then is set or cleared directly to a 1-bit condition. The pin needs external pull-up resistor.                                                                                                                                                                                                                                                                         |         |      |           |                                             |
| Host acknowledge output. In protocol A, the Decoder indicates that a read or write cycle is completed by asserting this output. In protocol B, the signal is used by the Decoder to indicate a read cycle that may be used by host flows. In protocol B, the pin may ignore the HDP30 signal.                                                                                                                                   |         |      |           |                                             |
| When this signal is deasserted it is de-asserted and then is reset. This pin needs an external pull-up resistor.                                                                                                                                                                                                                                                                                                                |         |      |           |                                             |
| Video Syncs and Clocks Interface (5 pins).                                                                                                                                                                                                                                                                                                                                                                                      |         |      |           |                                             |
| 127                                                                                                                                                                                                                                                                                                                                                                                                                             | VCLK    | 3-S  | IO (I)    | Reset: Standby: 3-S                         |
| Main video clock. 27.00MHz.                                                                                                                                                                                                                                                                                                                                                                                                     |         |      |           |                                             |
| 92                                                                                                                                                                                                                                                                                                                                                                                                                              | VCLK    | 3-S  | IO (I)    | Reset: Standby: 3-S (p.d.)                  |
| A division by five of the VCLK signal. This signal is used as a sync output.                                                                                                                                                                                                                                                                                                                                                    |         |      |           |                                             |
| 85                                                                                                                                                                                                                                                                                                                                                                                                                              | HSYNC   | 3-S  | IO (I)    | Reset: Standby: 3-S (p.d.)                  |
| Horizontal sync. Polarity and duration are programmable.                                                                                                                                                                                                                                                                                                                                                                        |         |      |           |                                             |
| 86                                                                                                                                                                                                                                                                                                                                                                                                                              | HSYNC   | 3-S  | IO (I)    | Reset: Standby: 3-S (p.d.)                  |
| Vertical sync. Polarity and duration are programmable.                                                                                                                                                                                                                                                                                                                                                                          |         |      |           |                                             |
| 87                                                                                                                                                                                                                                                                                                                                                                                                                              | VSNC    | 3-S  | IO (I)    | Reset: Standby: 3-S (p.d.)                  |
| Field indication. Polarity is programmable.                                                                                                                                                                                                                                                                                                                                                                                     |         |      |           |                                             |
| Analog Video Encoder Interface (7 pins).                                                                                                                                                                                                                                                                                                                                                                                        |         |      |           |                                             |
| 105                                                                                                                                                                                                                                                                                                                                                                                                                             | CDC(A)  | O    | AO        | Reset: Standby: 3-S                         |
| When the Decoder outputs composite video, this line is CVBS.                                                                                                                                                                                                                                                                                                                                                                    |         |      |           |                                             |
| 106                                                                                                                                                                                                                                                                                                                                                                                                                             | CDC(B)  | O    | AO        | Reset: Standby: 3-S                         |
| When the Decoder outputs RGB, this line is the Green output.                                                                                                                                                                                                                                                                                                                                                                    |         |      |           |                                             |
| 108                                                                                                                                                                                                                                                                                                                                                                                                                             | CDC(C)  | O    | AO        | Reset: Standby: 3-S                         |
| When the Decoder outputs RGB, this line is the Red output.                                                                                                                                                                                                                                                                                                                                                                      |         |      |           |                                             |
| 109                                                                                                                                                                                                                                                                                                                                                                                                                             | CDC(D)  | O    | AO        | Reset: Standby: 3-S                         |
| When the Decoder outputs RGB, this line is the Blue output.                                                                                                                                                                                                                                                                                                                                                                     |         |      |           |                                             |
| 103                                                                                                                                                                                                                                                                                                                                                                                                                             | CDC(E)  | O    | AO        | Reset: Standby: 3-S                         |
| When the Decoder outputs YUV, this line is the Y output.                                                                                                                                                                                                                                                                                                                                                                        |         |      |           |                                             |
| 104                                                                                                                                                                                                                                                                                                                                                                                                                             | CDC(F)  | O    | AO        | Reset: Standby: 3-S                         |
| When the Decoder outputs YUV, this line is the U output.                                                                                                                                                                                                                                                                                                                                                                        |         |      |           |                                             |
| 107                                                                                                                                                                                                                                                                                                                                                                                                                             | CDC(G)  | O    | AO        | Reset: Standby: 3-S                         |
| When the Decoder outputs YUV, this line is the V output.                                                                                                                                                                                                                                                                                                                                                                        |         |      |           |                                             |
| 101                                                                                                                                                                                                                                                                                                                                                                                                                             | RES     | I    | AI        | Reset: Standby: 3-S                         |
| Active-low load for gain adjustment of the DACs.                                                                                                                                                                                                                                                                                                                                                                                |         |      |           |                                             |
| 111                                                                                                                                                                                                                                                                                                                                                                                                                             | REF     | I    | AI        | Reset: Standby: 3-S                         |
| Voltage reference for gain adjustment of the DACs.                                                                                                                                                                                                                                                                                                                                                                              |         |      |           |                                             |
| 100                                                                                                                                                                                                                                                                                                                                                                                                                             | DO5W    | 3-S  | IO (p.d.) | Reset: output (low)<br>Standby: 3-S         |
| Compatible sync output. Active only when RGB analog output is selected. Otherwise, the signal is low.                                                                                                                                                                                                                                                                                                                           |         |      |           |                                             |
| Reset, Standby and Idle Status Interface (3 pins).                                                                                                                                                                                                                                                                                                                                                                              |         |      |           |                                             |
| 124                                                                                                                                                                                                                                                                                                                                                                                                                             | RESET   | I    | Input     |                                             |
| Reset input. Once de-asserted, the Decoder starts the initialization process.                                                                                                                                                                                                                                                                                                                                                   |         |      |           |                                             |
| 122                                                                                                                                                                                                                                                                                                                                                                                                                             | STANDBY | I    | Input     |                                             |
| Standby input. When asserted together with RESET, all outputs and bidirectional pins float, such that the Decoder is electrically disconnected from the interface. All internal clocks are disabled, and the power consumption is minimized.                                                                                                                                                                                    |         |      |           |                                             |
| 160                                                                                                                                                                                                                                                                                                                                                                                                                             | RES     | 3-S  | IO (p.d.) | Reset: output (high)<br>Standby: 3-S (p.d.) |
| Idle, Tri-state and Reset status indication output.                                                                                                                                                                                                                                                                                                                                                                             |         |      |           |                                             |
| Host Interface (29 pins).                                                                                                                                                                                                                                                                                                                                                                                                       |         |      |           |                                             |
| 2                                                                                                                                                                                                                                                                                                                                                                                                                               | HDP10   | I    | Input     |                                             |
| Determines the width of the host interface data bus. It is allowed to be changed only during RESET. A low level (GNP1) configures the Decoder to an 8-bit host data interface. A high level (HNP1) to 16-bit mode.                                                                                                                                                                                                              |         |      |           |                                             |
| Determines the order of bits on the host interface data bus. In case of 1-bit width (HNP1 data bus), it is allowed to be changed during RESET. A low level (GNP2) configures the Decoder to a high level (HNP2) data bus. In case of 16-bit width (HNP1) it is equivalent to the 1-bit bus. In case of 16-bit width (HNP1) it is equivalent to the 1-bit bus. In case of 16-bit width (HNP1) it is equivalent to the 1-bit bus. |         |      |           |                                             |
| 4                                                                                                                                                                                                                                                                                                                                                                                                                               | HDP10   | I    | Input     |                                             |
| Determines the protocol type for 1-bit and 16-bit mode host interface. It is allowed to be changed only during RESET. A low level (GNP3) configures the Decoder to type A. A high level (HNP3) to type B.                                                                                                                                                                                                                       |         |      |           |                                             |

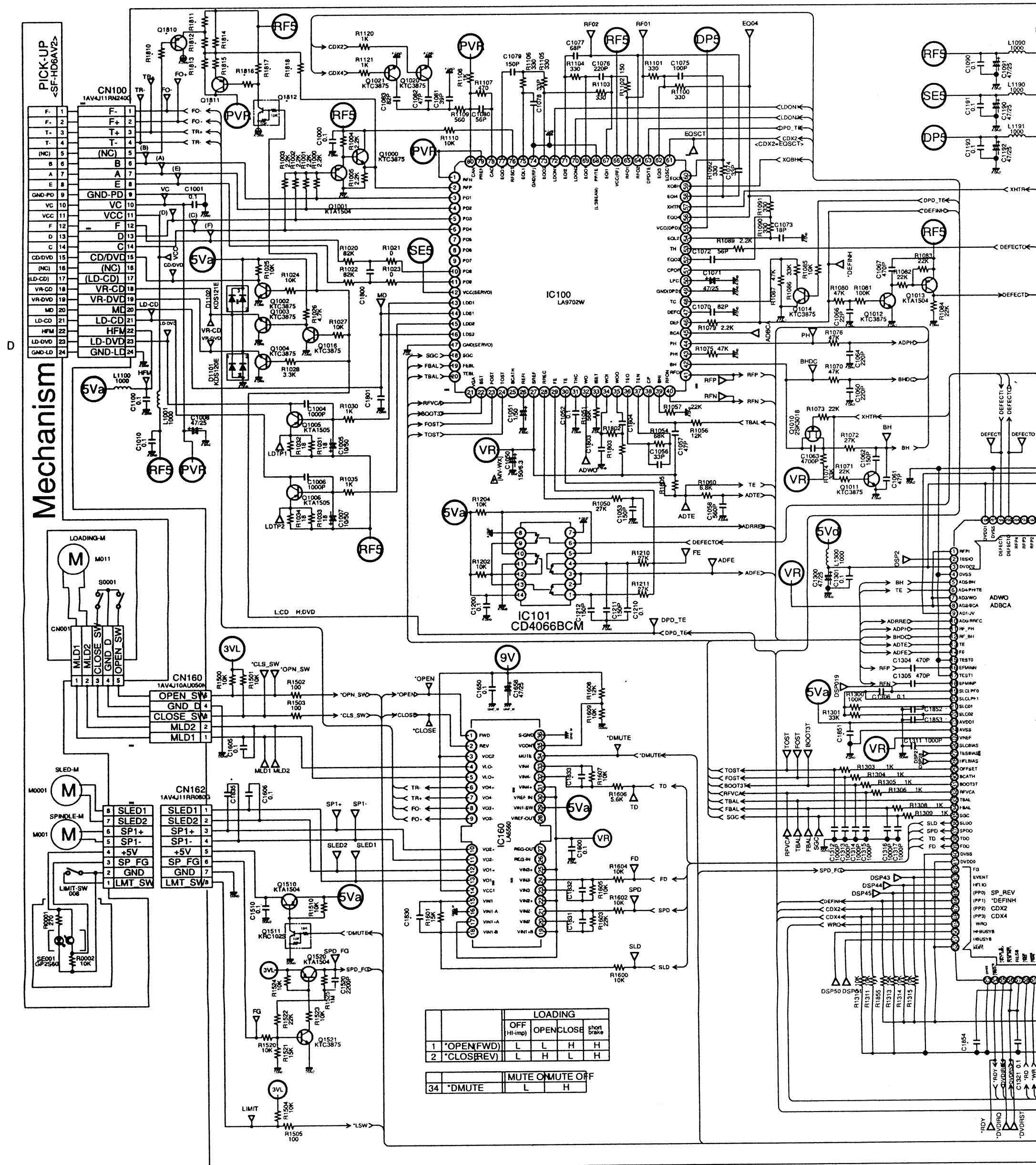
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This is a basic block diagram.



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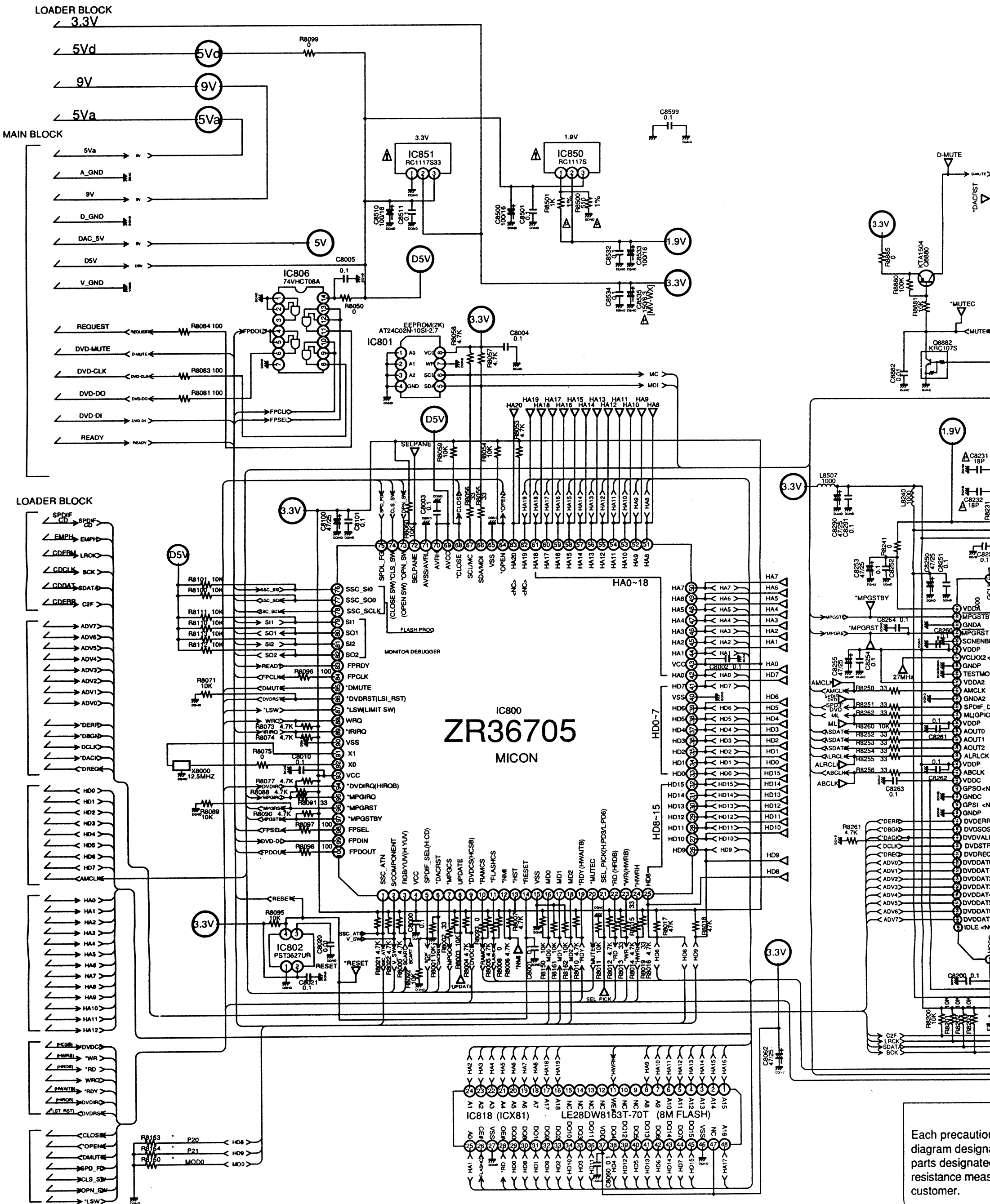


This is a basic schematic diagram.



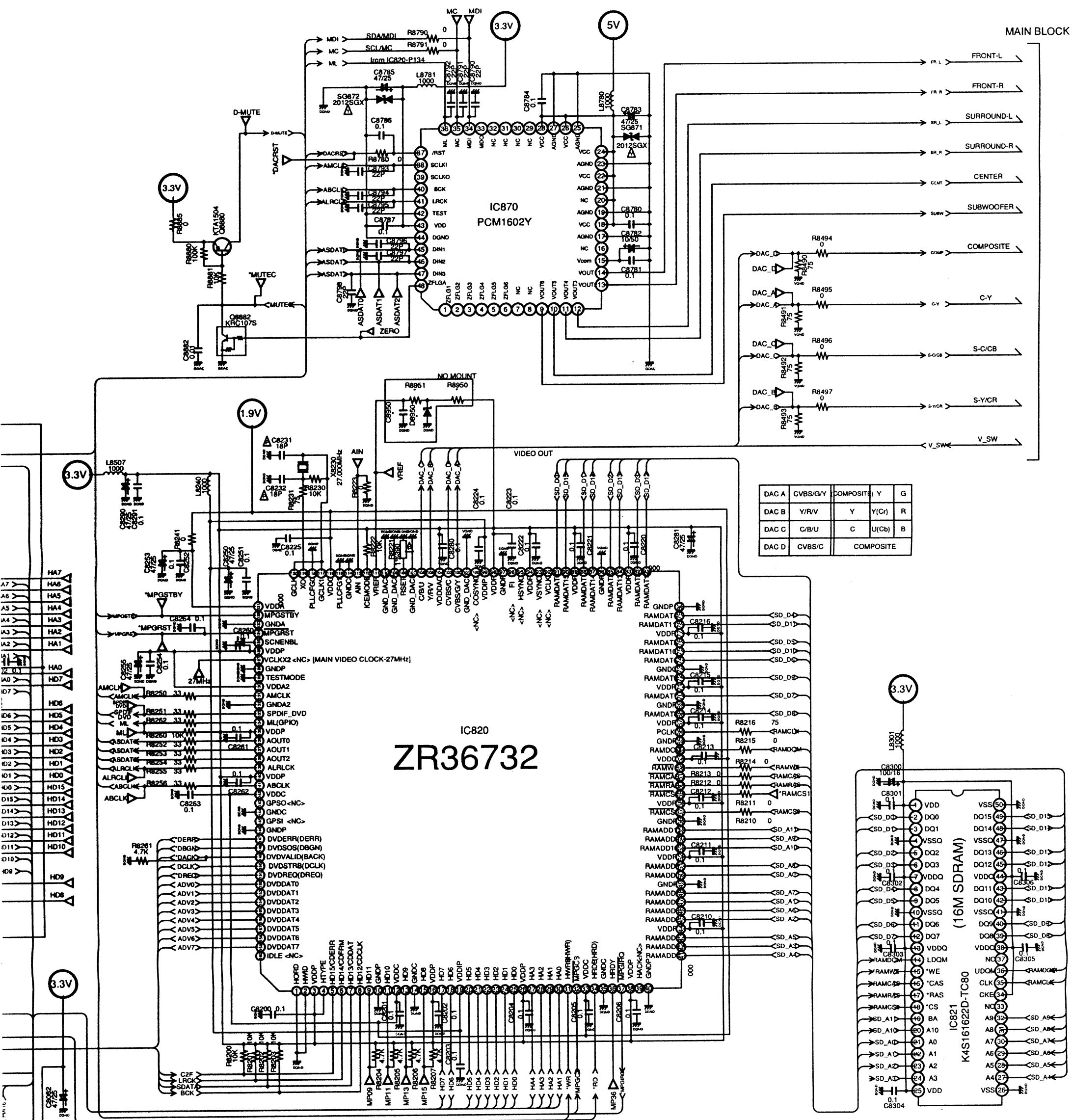


## SCHEMATIC DIAGRAM (MPEG)



Each precaution diagram designates parts designated resistance measures to the customer.

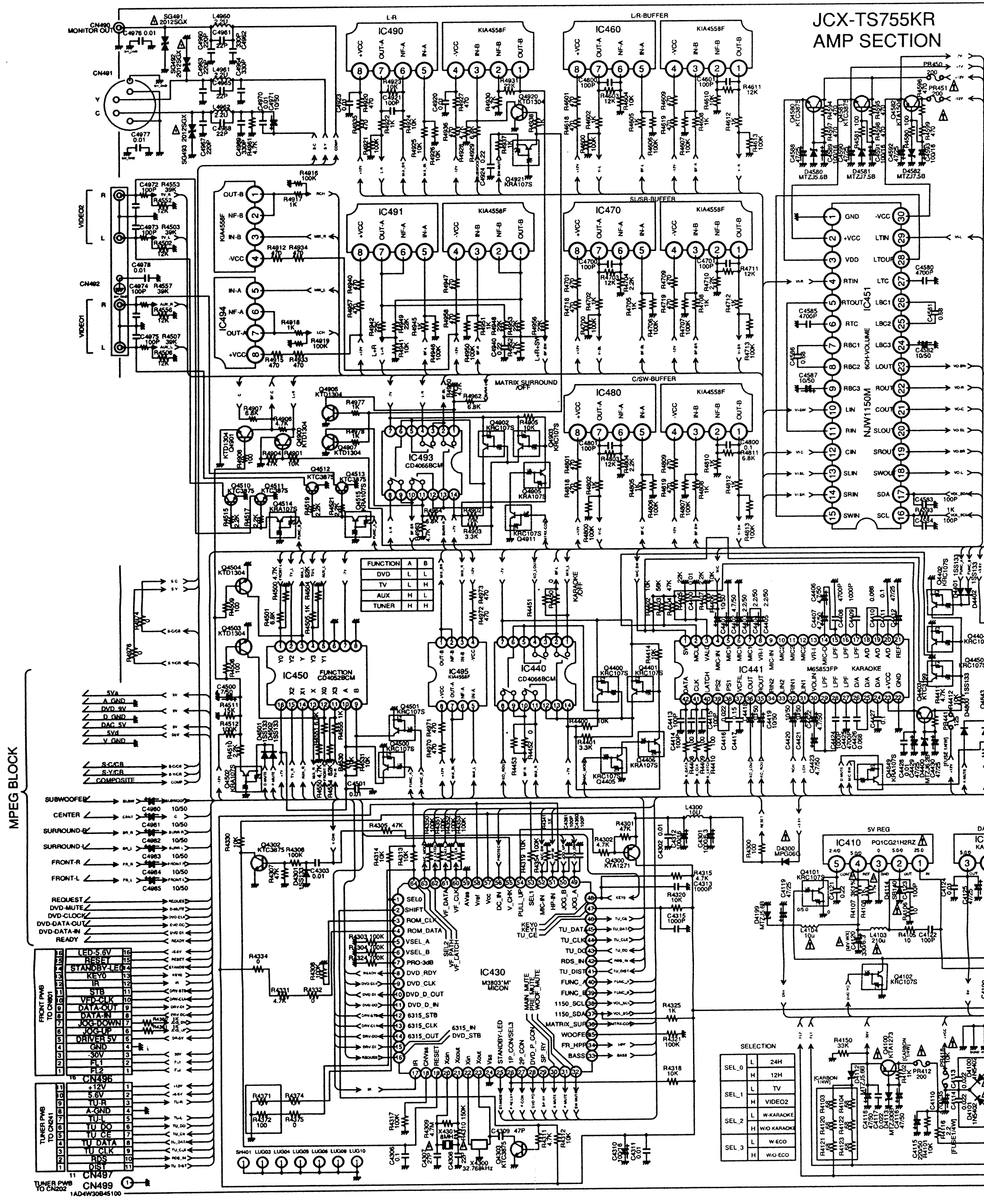




# PRODUCT SAFETY NOTICE

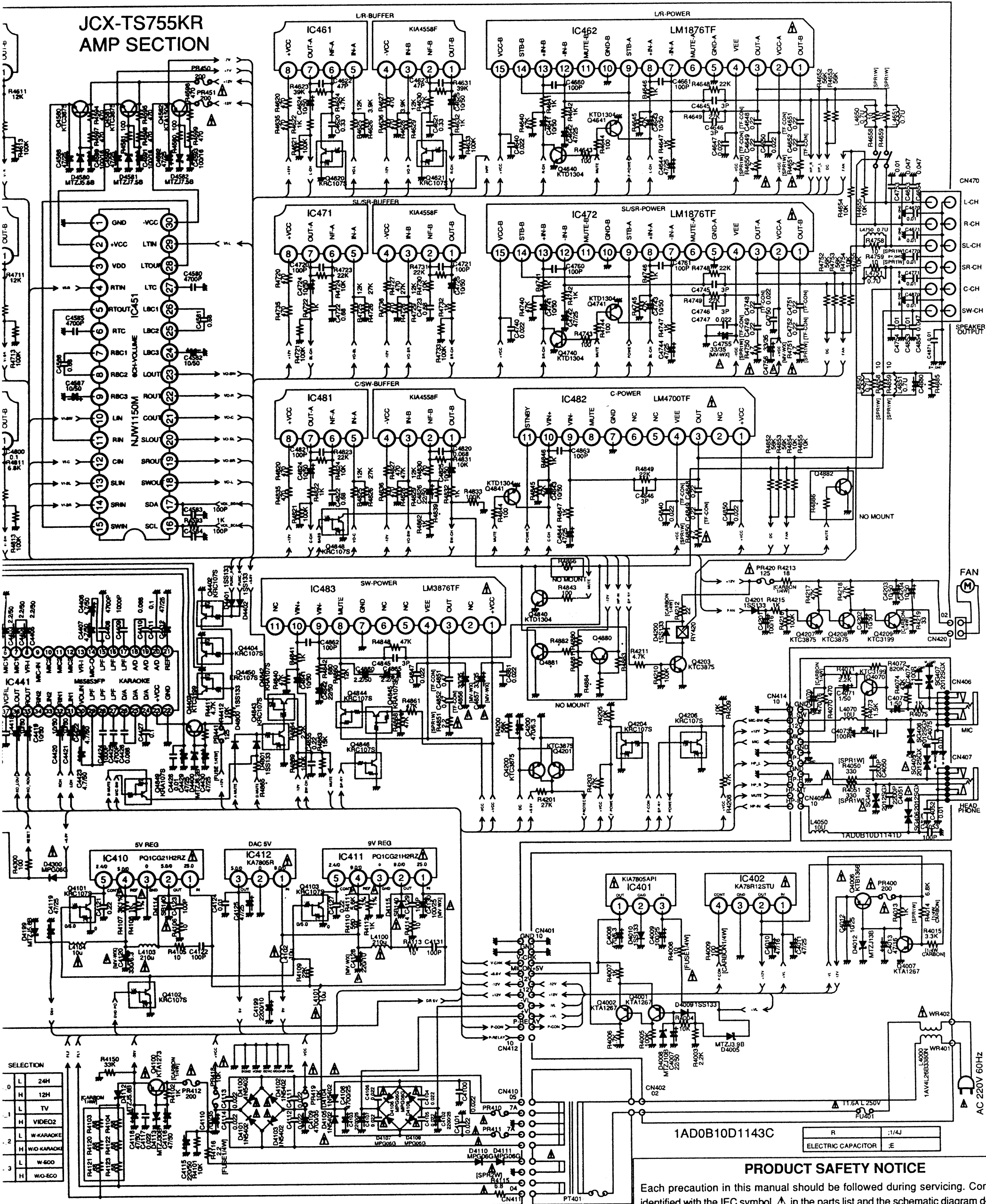
Each precaution in this manual should be followed during servicing. Components identified with the IEC symbol  in the parts list and the schematic diagram designated components in which safety can be of special significance. When replacing a component identified by , use only the replacement parts designated, or parts with the same ratings of resistance, wattage or voltage that are designated in the parts list in this manual. Leakage-current or resistance measurements must be made to determine that exposed parts are acceptably insulated from the supply circuit before returning the product to the customer.

# SCHEMATIC DIAGRAM (AMP)



This is a basic schematic diagram.

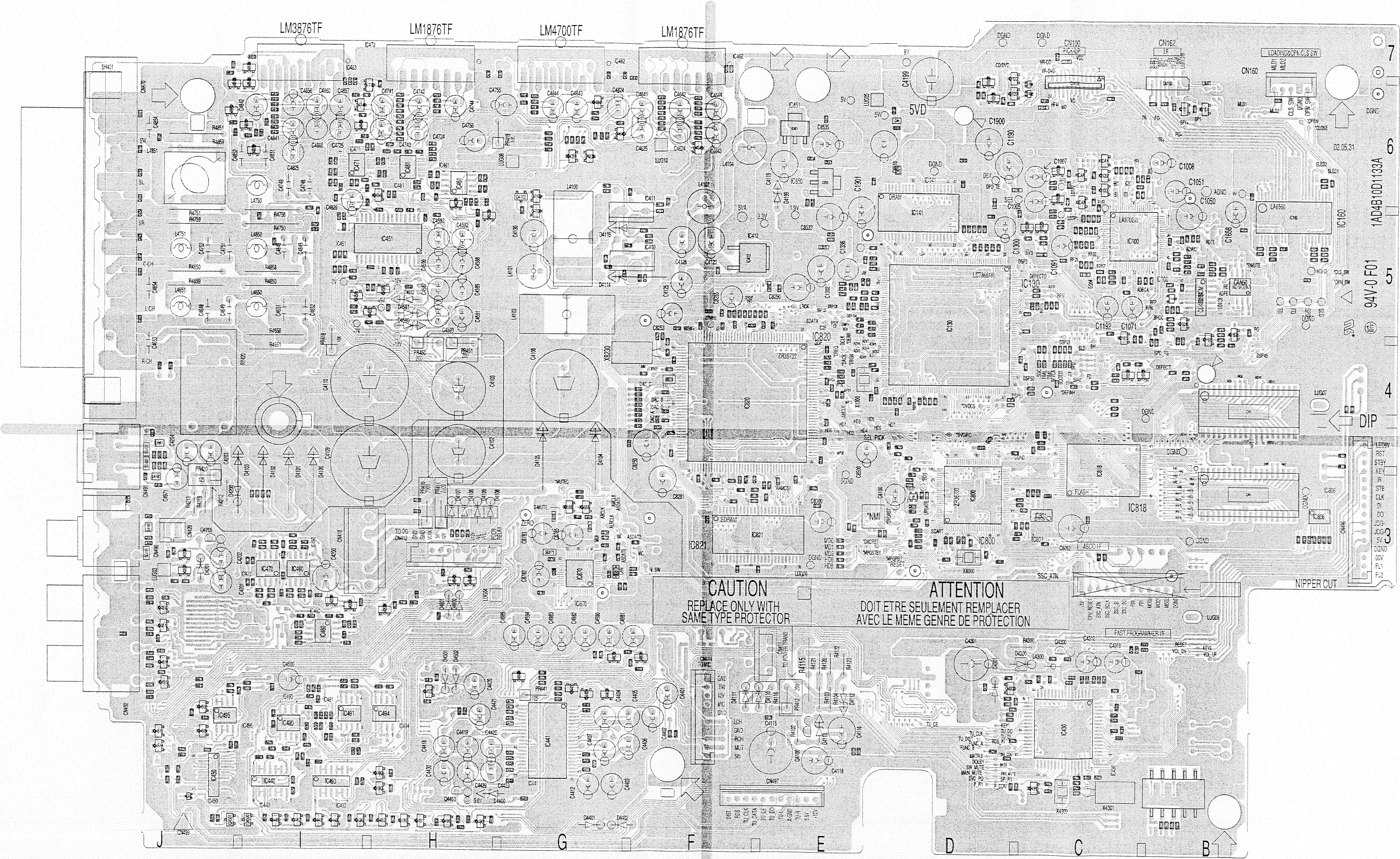
# JCX-TS755KR AMP SECTION



## PRODUCT SAFETY NOTICE

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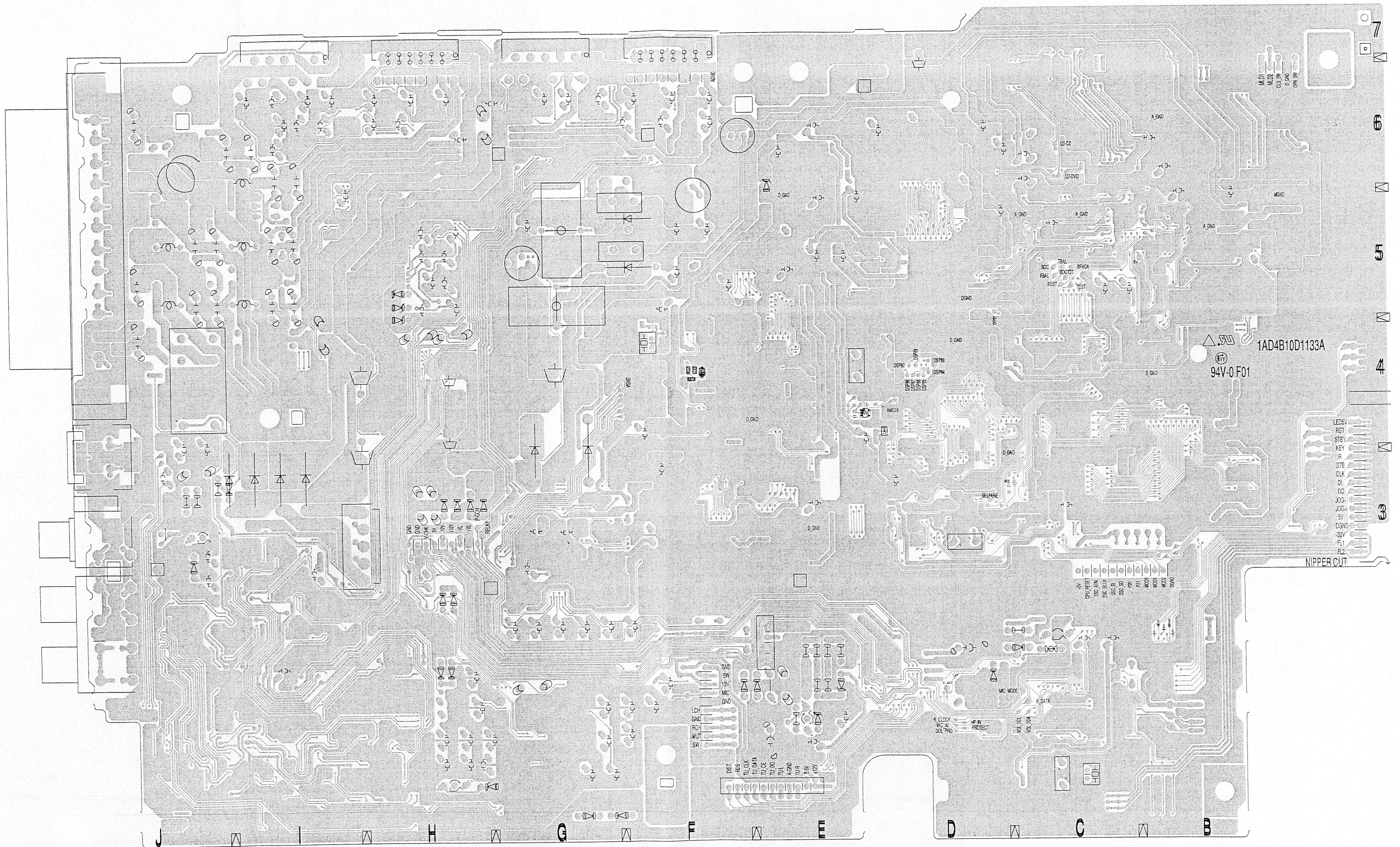








## WIRING DIAGRAM (MAIN,AMP-DVD B SIDE)





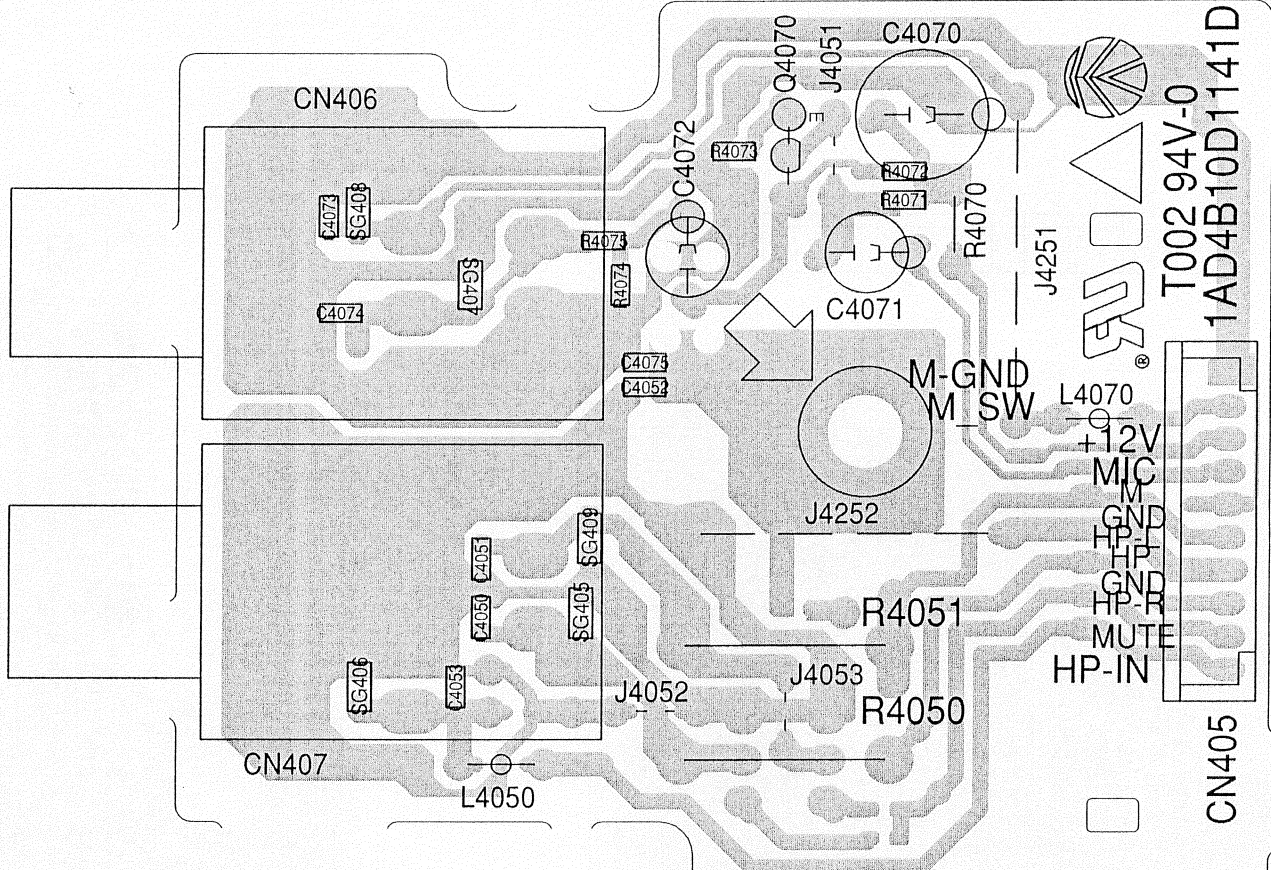
Connector Table:

| Connector | Signal  |
|-----------|---------|
| CN201     | DIST    |
|           | RDS     |
|           | TU_CLK  |
|           | TU_DATA |
|           | TU_CE   |
| CN202     | TU_DO   |
|           | TU_L    |
|           | A_GND   |
|           | TU_R    |
|           | 5.6V    |
| CN203     | +12V    |

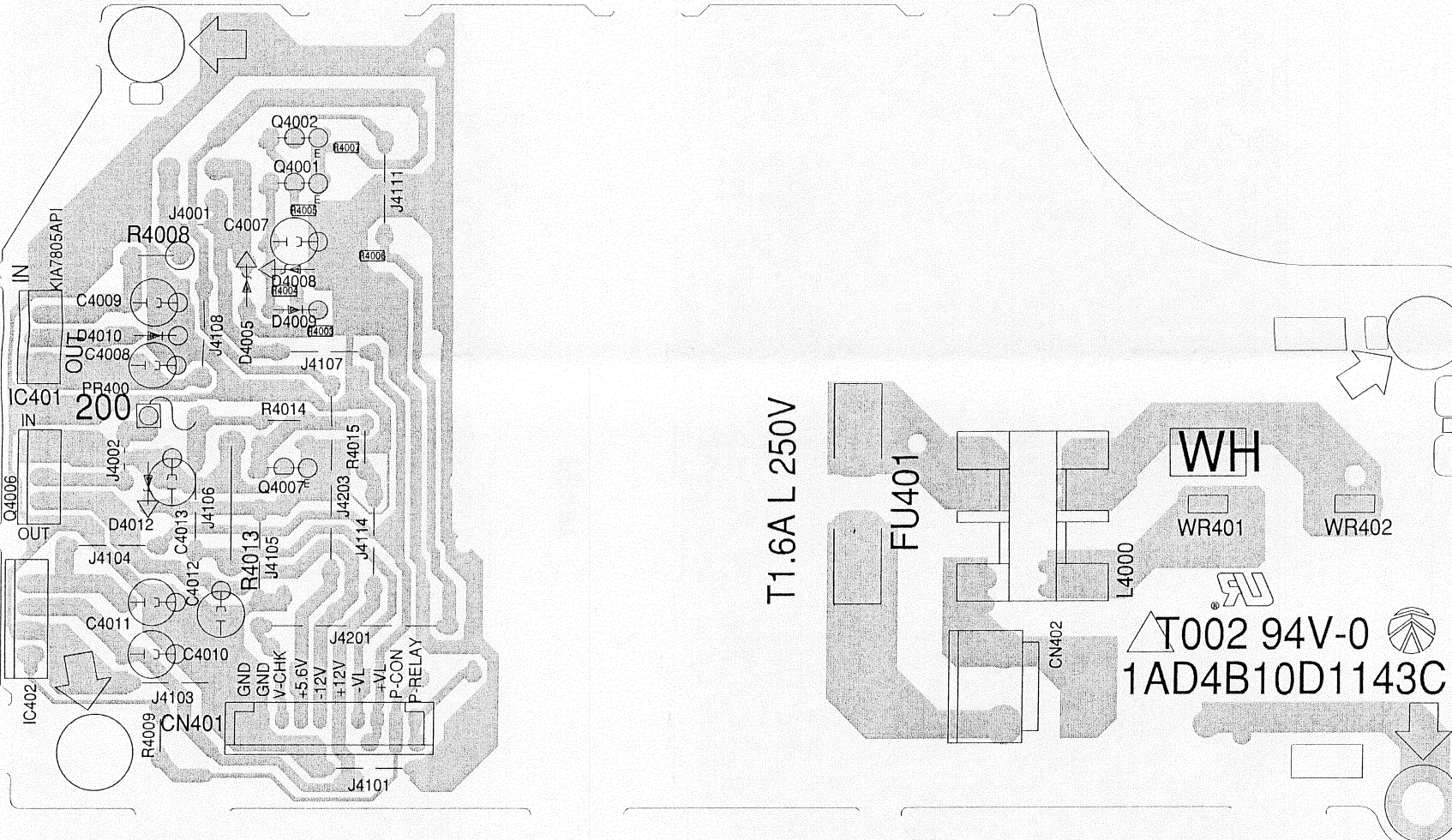
- 58 -



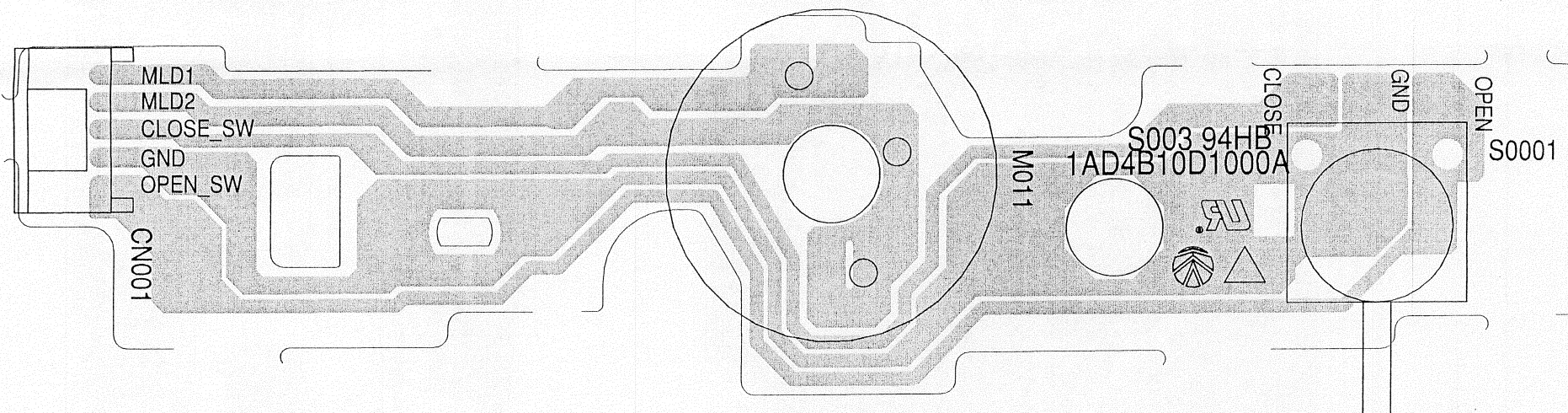
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## HEADPHONE

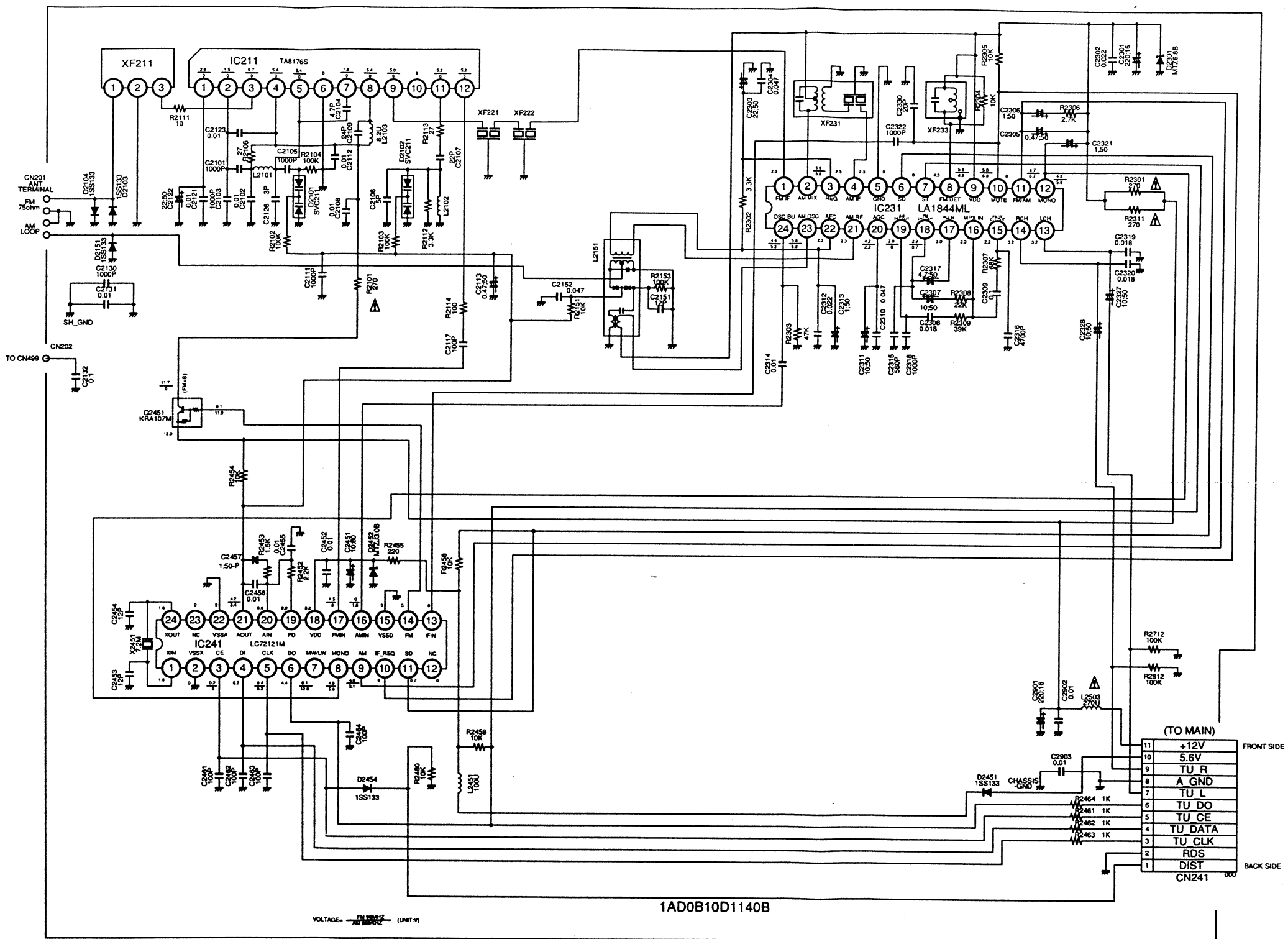
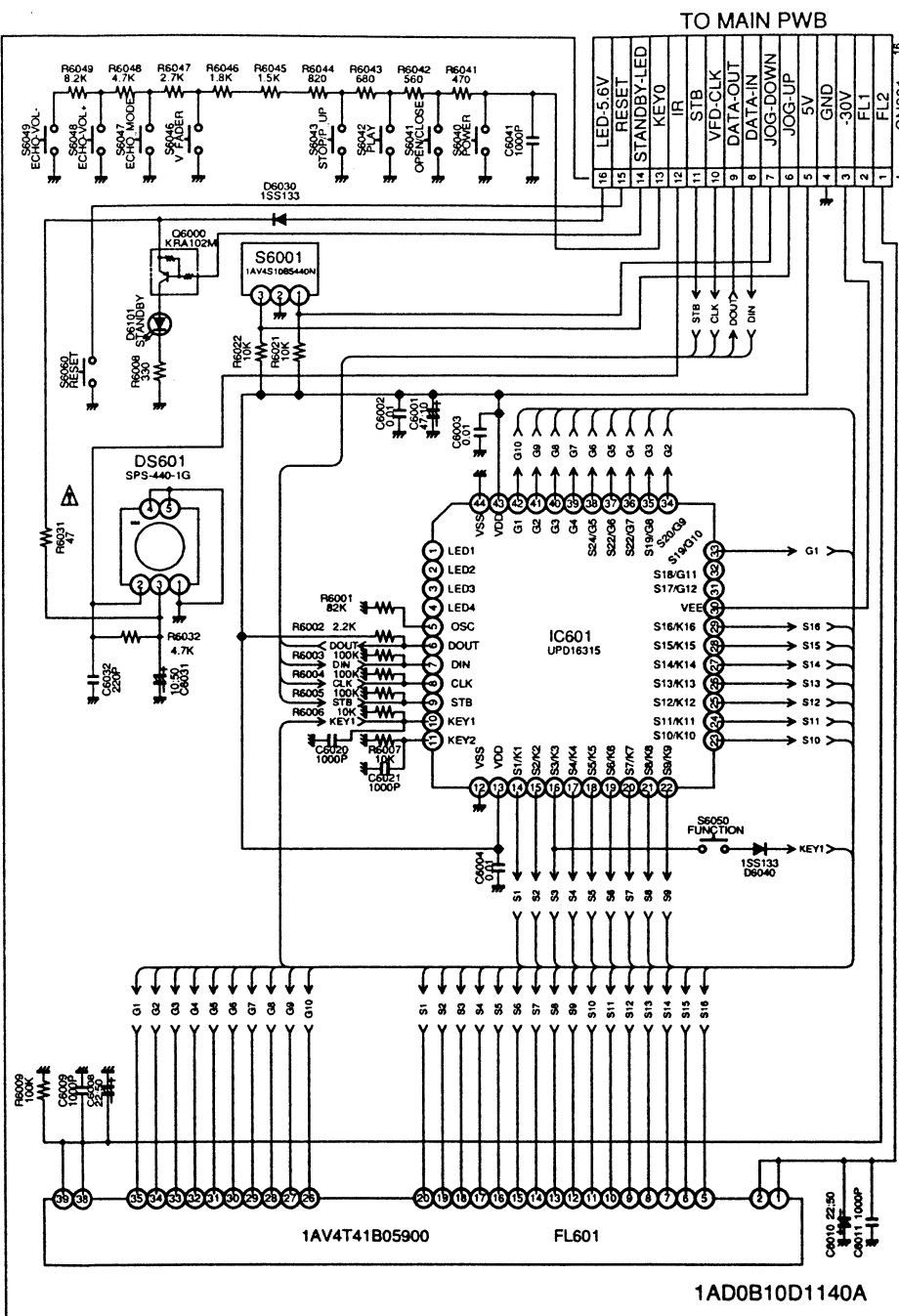


## POWER SUPPLY



## MECHA SW

### SCHEMATIC DIAGRAM (FRONT , TUNER)

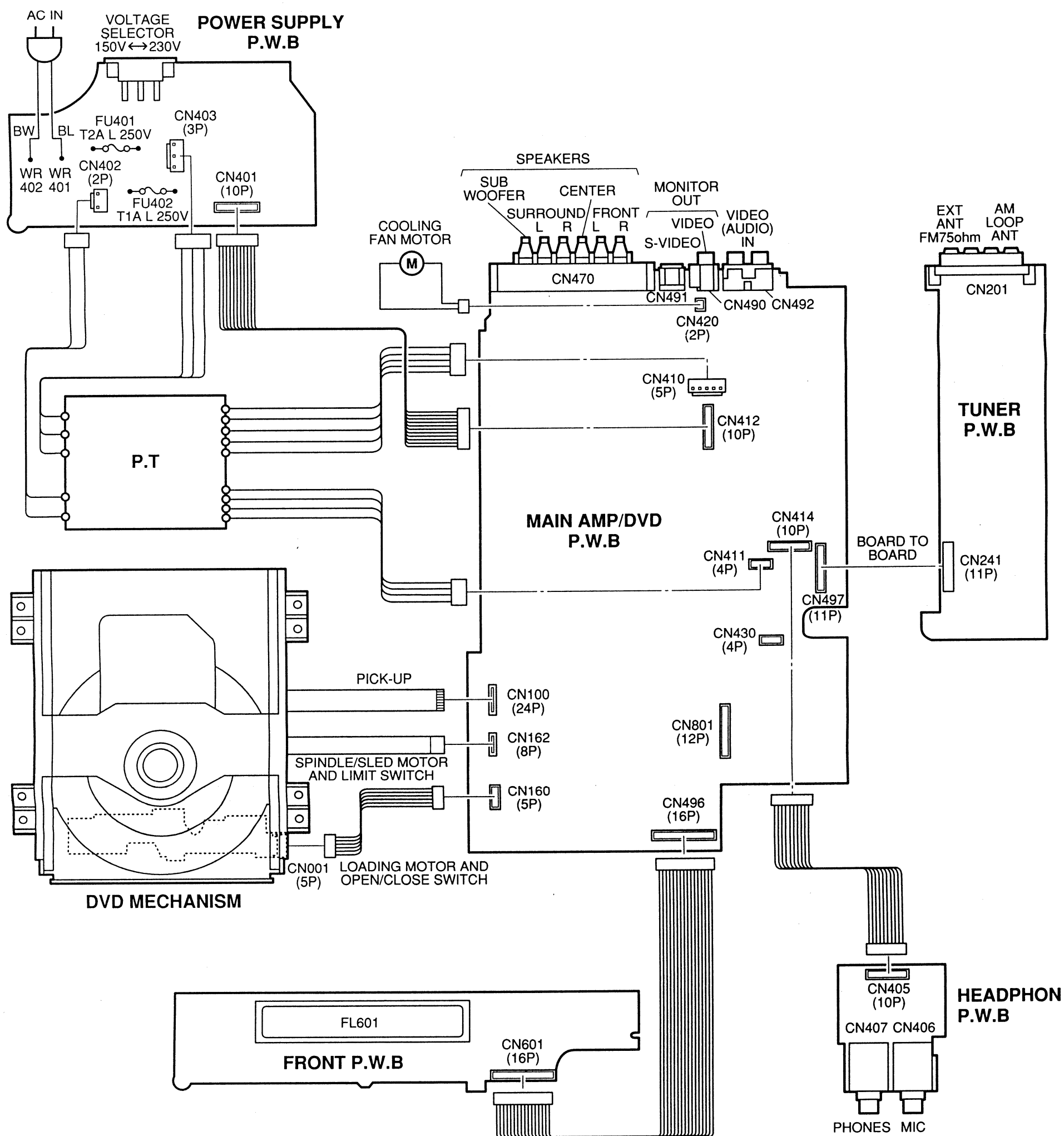


## PRODUCT SAFETY NOTICE

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# WIRING CONNECTION



This is a basic wiring connection.

**SANYO**

SANYO Electric Co., Ltd.  
OSAKA, JAPAN